Analysis of Electrolytic Capacitor Degradation under Electrical Overstress for Prognostic Studies

Jason Renwick[1], Chetan S. Kulkarni[2], and José R. Celaya[3]

[1] *University of West Indies, St. Agustine, Trinidad and Tabago*
jasondren@gmail.com

[2] *NASA Ames Research Center (SGT Inc.), Moffett Field, CA, USA*
chetan.s.kulkarni@nasa.gov

[3] *Schlumberger, Software Technology and Innovation Center, Menlo Park, CA, USA*
JCelaya@slb.com, jose.r.celaya@nasa.gov

ABSTRACT

The implementation of prognostics methodologies to electrical and electronics components and systems has become essential and critical as these systems find more prominence recently as they replace traditional systems in several critical applications. There are several challenges due to great variety of components used in a system, a continuous development of new electronics technologies, and a general lack of understanding of how electronics fail. Traditional reliability techniques in electronics tend to focus on understanding the time to failure for a batch of components of the same type. In this work we discuss degradation in electrolytic capacitors which are part of power supplies and are very crucial in their operation. We discuss our experimental setup and further present our findings related to the degradation observed in these capacitors under accelerated electrical aging under different operating conditions. The understanding of the time dependent degradation process is critical for the development of model based prognostics algorithms which provide a continuous condition-based estimation of the remaining useful life of the device under test.

1. INTRODUCTION

The development of prognostics methodologies for electrical and electronics field has become more important as more of these systems are being used to replace traditional systems in several applications in fields like aeronautics, maritime, and automotive (Saha, Goebel, & Christophersen, 2009). The implementation of this methodology presents several challenges due to great variety of components used in a system, a continuous development of new electronics technologies, and a general lack of understanding of how electronics fail. Traditional reliability techniques in electronics tend to focus on understanding the time to failure for a batch of components of the same type. Just until recently, there has been a push to understand, in more depth, how a fault progresses as a function of usage, namely, loading and environmental conditions.

Electrolytic capacitors have become critical components in electronics systems in several domains. They are known for their low reliability and frequent breakdown in critical systems like power supplies of avionics equipment and electrical drivers of electro-mechanical actuators. Capacitors are used as filtering elements on power electronics systems. Electrical power drivers for motors require capacitors to filter the rail voltage for the H-bridges that provide bidirectional current flow to the windings of electrical motors. These capacitors help to ensure that the heavy dynamic loads generated by the motors do not perturb the upstream power distribution system (Kulkarni, Biswas, Koutsoukos, Goebel, & Celaya, 2010; Orsagh, Brown, Roemer, Dabnev, & Hess, 2005).

In this work we establish the hypothesis that tau (τ), the RC time constant on a RC type filter circuit is a good precursor of failure candidate for prognostics. The degradation process in a capacitor must be reflected in this quantity. Degradation in the capacitors is observed by accelerated aging the devices under higher electrical stress. A charge/discharge square wave is applied to the devices and health is monitored by logging the charge/discharge cycles at regular intervals. Furthermore, we propose a way to estimate τ through the rise time observation of the charge transient in a capacitor.

The rise time tau value of the charge cycle is calculated based on which the degradation is observed. In addition electro impedance spectroscopy (EIS) measurements are also taken

to compute the values of Capacitance (C) and equivalent series resistance (ESR). The tau value calculated from the rise time and EIS measurements are used for studying the degradation in the test devices.

The papers discusses our research work in the following sections. Section 2 discusses the research methodology which we are following to study degradation in the capacitors and previous work. Section 3 discuss the experimental setup for the accelerated aging experiments. The paper concludes with discussion on results observed and next steps.

2. RESEARCH METHODOLOGY

Our research goal for this work is focused on studying the degradation process from an accelerated life test on real electrolytic capacitors. In the experiments, commercial-off-the-shelf capacitors are subjected to electrical stress conditions in order to observe and record the degradation process and identify performance conditions in the neighborhood of the failure criteria in a considerably reduced period.

2.1. Failure Precursor

The devices under test are subjected to charge/discharge waveforms at different voltage levels. In earlier work Electro-impedance spectroscopy was used periodically during the experiment to characterize the frequency response of the capacitor. These measurements along a reduced order model based on passive electrical elements are used to identify the capacitance and parasitic resistance element of the device.

As the capacitance and resistance of the device changes, these are reflected in the RC time constant (τ) values. The RC time constant, also called tau (τ), is the time constant of an RC circuit, is equal to the product of the circuit resistance (Ω) and the circuit capacitance (μ). We implement a methodology to observe degradation at the component level based on the rise time during charging. The capacitors are cycled from 0 to a threshold stress voltage in a 10 second charge/discharge cycle continuously and these cycles are recorded. This recorded data is used to study and interpret the degradation occurring in the devices.

Though with the EIS measurements we compute C and ESR values based on the system identification methods, there are some disadvantages of EIS measurement methods at the component level which are listed as below.

- The measurements cannot be taken inline of the circuitry and the test device has to be removed for measurement.
- Measurement noise is observed.
- Study degradation based on the output waveforms.
- Equipment availability to take EIS measurements. There is a requirement of specific instrument to take the measurements.

2.2. Previous Work

We studied accelerated degradation under electrical stress (Celaya, Kulkarni, Biswas, & Goebel, 2011; Celaya, Kulkarni, Goebel, & Biswas, 2012) as well as thermal stress (Kulkarni, 2012) in electrolytic capacitors . A preliminary approach to remaining useful life prediction of electrolytic capacitors was presented in (Celaya et al., 2011). This paper here builds upon the work presented in the preliminary remaining useful life prediction in (Celaya et al., 2012).

In earlier work of a physics based degradation model during the accelerated life test a Bayesian framework was implemented to estimate the state of health of the capacitor based on measurement updates of key capacitor i.e, capacitance and ESR parameters. Unscented Kalman Filter (UKF) algorithm is used to track the state of health and the degradation model is used to make predictions of remaining useful life once no further measurements are available. A discussion and physical interpretation of the degradation model is presented (Celaya et al., 2011, 2012).

Earlier work focused on implementing prognostics methodologies to data collected at component level. Usually in field applications it is difficult to measure component level data. Our approach in this work is to collect system level measurements and compare them with component level measurements so as to study and apply prognostics methodologies at system level.

3. ACCELERATED AGING EXPERIMENTS

Accelerated life test methods are often used in prognostics research as a way to assess the effects of the degradation process through time. It also allows for the identification and study of different failure mechanisms and their relationships with different observable signals and parameters. In the following section we present the accelerated aging methodology and an analysis of the degradation pattern induced by the aging. The capacitors are subjected to three voltage levels and their degradation was observed over the period of aging time. In this work we discuss specifically aging of the devices at 10V which is one of the voltage levels to which the devices were subjected for accelerated aging.

Capacitors were subjected to high voltage stress through an external supply source using a specifically developed hardware as described by block diagram in Fig. 1. To monitor the degradation of the devices measurements were taken on each of the devices. The first is the online monitoring which captures the voltage and current signature while the other is based on the EIS measurements. The schematic shown in Fig.1 shows the measurements taken for each capacitor.

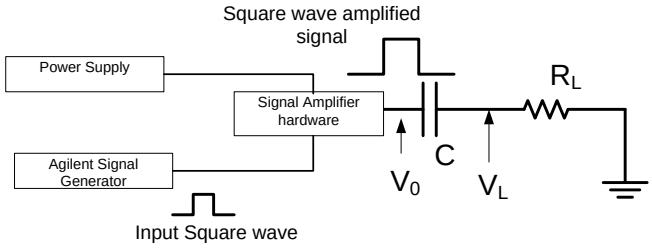

Figure 1. Developed Hardware Board Schematic Diagram

3.1. Experiments

For this experiment a batch of 7 capacitors of 2200μF capacitance each are used. A hardware pcb board was developed which would subject the devices under test to different voltage conditions. The voltage conditions were selected such that it would stress the devices above their normal operating range as mentioned by the manufacturer. The capacitor components under test are maximum rated voltage of 10V, maximum current rating of 1A and maximum operating temperature of 85°C were used for the study. Under normal operating conditions the devices usually are used for a DC-DC converter with a output of 5V and ripple of less than 1% over its operating range. The boards subject the capacitors to electrical stress condition under 10V, 12V and 15V which is well above their normal operating range. This will stress the devices and we are able to observe and monitor the degradation in the devices within a short time period. Fig. 2 shows the complete setup of the experiments with the developed hardware and data measurement using NI LabView.

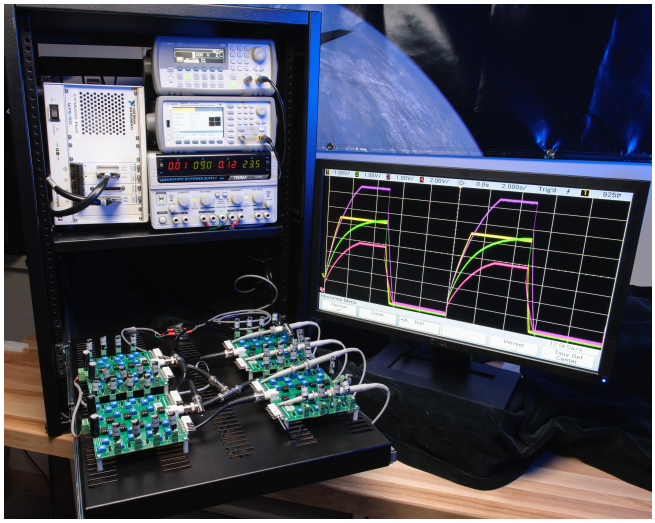

Figure 2. Actual Experiment Setup with developed boards.

As shown in Fig. 1 each device is subjected to a square waveform of a specific voltage level. This simulates the charge/discharge cycle for the capacitor. The charge/discharge cycle is set such that the device is charged at the particular voltage level and the charge is held steady for a brief period of time before it is discharged through a constant load of 100 Ω. The continuous charge/discharge cycles subjects the devices to a high stress which leads to degradation. Due to the charging/discharging cycle the internal temperature of the capacitor increases which leads to changes in the capacitance and internal series resistance parameters of the device. Details of the theory is discussed in (Kulkarni, Biswas, Koutsoukos, Celaya, & Goebel, 2010).

3.1.1. Online Measurements

For the online measurements, charge/discharge waveforms are captured at every 10 minutes segments in burst of 10 cycles. Since we do not anticipate any change every minute due to the stressed conditions, the measurements are taken every 10 mins. These are done through a developed NI Labview integrated software and hardware system. A NI acquisition hardware system is used for collecting the data from the different boards and a developed LabView GUI is used to control the hardware. In addition a function generator is used to generate the required amplitude and frequency waveform to age the devices. As shown in Fig. 1 both the V_O and V_L measurements are captured to calculate the rise time (τ) during each cycle. As per our hypothesis as the devices degrade we will observe the value of τ decrease over the period of time. The plots in Fig. 3 show V_O transients for one of the capacitors (Capcitor #5) on the board as it ages over the period of time due to electrical stress. The plot also shows the corresponding change in V_L values as the capacitor degrades. (Note: There are no legends for Fig. 3 since the V_L and V_O are plotted over the entire aging data). As discussed earlier the τ value is calculated based on the rise time of V_L, which changes over the operating age as seen in Fig. 3. The τ value is calculated offline at regular intervals to monitor how the device has been performing due to the stress conditions. τ calculations for all the devices on board are done, the results of which are discussed later in the sections.

3.1.2. EIS Measurements

The SP-150 Biologic SAS impedance measuring instrument uses Electrochemical Impedance spectroscopy, and finds applications in corrosion, battery, fuel cell development, sensors, and physical electro-chemistry. Impedance measurements can be made in a potentiostatic mode or in a galvanostatic mode. The PEIS mode is used for characterizing all the capacitors under test. Electrochemical impedance spectroscopy measurements are available to characterize the electrical performance of the capacitor under test.

The ESR and capacitance values were estimated from the capacitor impedance frequency response measured using the EIS instrument as shown in the plots of Fig. 4. During each measurement the voltage source was shut down, capac-

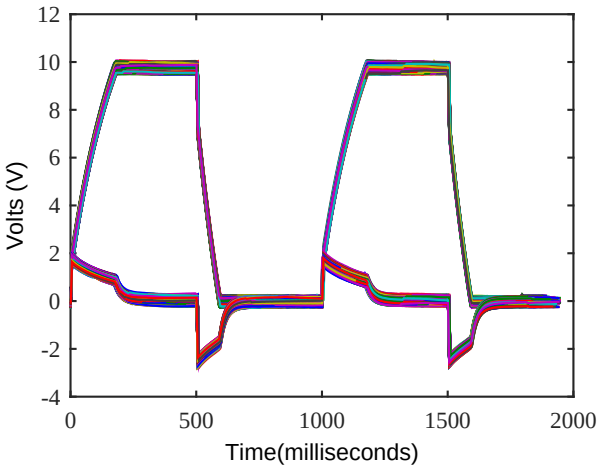

Figure 3. Transient plots at different aging times for capacitor # 5 (10V Board)

itors were discharged completely and then the characterization procedure was carried out. This process is discussed in (Celaya et al., 2012).

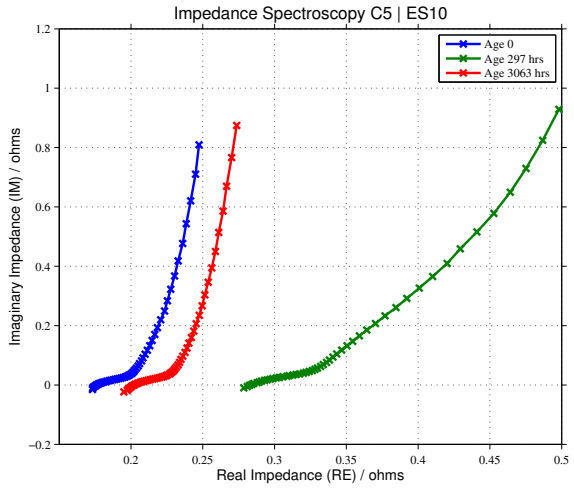

Figure 4. EIS measurements plots at different aging times : Cap C5

4. RESULTS

In this section we discuss degradation data observed in devices under test for the experiments performed. Plots in Fig. 4 show the impedance measurement for one of the devices under test. The figure plots the imaginary and real values for a spectrum of frequencies. Using a system identification model C and ESR values are retrieved from the measured raw data. As can be seen from the plots, as the device ages the slope of the measurement values changes. This is due to the change in the C and ESR values which change with the aging of the device.

Table 1 shows the values of C and ESR for all the devices aged on the board. It can be observed that the C values for all the devices cross a soft threshold point of 20% below the actual capacitance values. Usually a capacitor is considered not fit for use if its capacitance reaches 20% below its initial values (MIL-C-62F, 2008; IEC-60068-1, 1988). Though the devices crossed the threshold we continued the experiments to study any further effects on the internal structure of the device to high electrical stress. It was observed that the capacitance values increase after around 400 hours of operation under the continuous charge/discharge cycle at 10V.

The change in the capacitance value beyond 400 hours could be hypothesized to the oxide layer formation phenomenon which may lead to formation of a parallel capacitance. We are currently studding the data and the underlying physics phenomenon models to know more about this change in the capacitance value increasing after crossing the failure threshold.

In addition to the EIS measurements we also tracked the degradation of the devices through online measurements during the charge/discharge cycles. As the capacitor degrades, computed RC time constant from the charge cycle during the charge/discharge cycle changes given by $\hat{\tau}(t)$ is constant. As the device degrades the C and ESR values change and this affects the RC time constant of the device. As the C and ESR values change the RC time constant changes affecting the change in the $\hat{\tau}(t)$ values.

For this work the online measurements were not started until upto around 1100 hours into the aging of the devices. As can be seen from the plots in Fig. 5

The two methods used to calculate $\hat{\tau}(t)$ require i) offline measurements and ii) online measurements. In our previous work (Celaya et al., 2011, 2012) EIS measurements (offline) was seen as the ground truth when estimating capacitor parameters. The opposing method (online) comes from calculation done to the transient voltage data collected. Fig. 6 is a comparison of the online to offline values of tau. Although these values have a comparable trend, they exhibit a distinct difference in magnitude.

This observed difference can be attributed to a number of factors related to the physical experimental set-up, operating temperatures and circuit modeling. The implication of the opposing methods (offline vs. online) is that the measurements are taken at different temperature i.e. operating temperature opposed to resting temperature (room temperature). As seen in previous work (Kulkarni, Biswas, Celaya, & Goebel, 2013) one of the most significant factors that impact capacitor degradation is temperature.

Table 1. C and ESR computed values at different aging times for 10V Board

Device	Age : 0 hrs		Age : 296 hrs		Age : 3063 hrs	
	Cap (μF)	ESR (Ω)	Cap (μF)	ESR (Ω)	Cap (μF)	ESR (Ω)
1	1942.4	1859.0	1521.8	3370.0	1838.8	2068.6
2	1943.0	1901.0	1541.8	3578.4	1809.8	2140.8
3	1930.6	1788.8	1500.0	3264.2	1798.0	2009.4
4	1857.6	1901.8	1495.6	3252.6	1720.0	2351.2
5	1931.0	1877.2	1481.8	3226.0	1795.4	2139.2
6	1926.2	1919.8	1512.6	3259.6	1796.8	2019.2
7	1899.6	1906.0	1482.0	3244.4	1755.0	2226.6

With regards to the experimental setup, the transient voltage data is collected by NI hardware with supporting LabVIEW software whereas the EIS data is collected by different hardware (SP-150 Biologic). A major effect difference in hardware may have is the calibration standards. By using offline EIS measurements we also change the circuit under which the capacitor is being observed, whereas, if the transient data is measurement online, the capacitor circuit will see the effects of the connected hardware. It would be very difficult to determine the effect that the measurement hardware has on a circuit. When determining the capacitor characteristics from the EIS measurements we apply a circuit model to the data and extract a value for capacitance and ESR. We currently use a simplified lumped parameter model (C + ESR) when analyzing EIS data. One option to explain is that our model of the capacitor is no long accurate to the capacitors under test. As capacitors are left unused or while in use, their physical/chemical composition may change hence a simple C+ESR lumped parameter model may be obsolete in the later stages of aging.

5. CONCLUSION AND DISCUSSION

The results presented show that by measuring the τ value of a capacitor may be a viable way of observing a capacitor's degradation. Also, by using $\hat{\tau}$(t) as the observed parameter we can develop online methods of characterizing capacitors and a metric to calculate remaining useful life or end of life of capacitors still in use. The practicability of doing offline measurements is very low when trying to integrate into a system hence doing online measurements would allow for more integration into electronic systems.

If a generic model is derived for a capacitor based on its $\hat{\tau}$(t) values, it may be possible to define the EOL of a system (based on capacitor failure) based on its circuit design i.e. the components possibly affecting the tau measurements.

ACKNOWLEDGMENTS

The authors would like to gratefully acknowledge the contributions of researchers at NASA Ames Research Center: Kai Goebel and Scott Poll. The funding for this research is provided by NASA ARMD System-wide Safety & Assurance Technology (SSAT) project. The work was done by José R. Celaya while working at the Prognostics Center of Excellence, NASA Ames Research Center.

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BIOGRAPHIES

Jason Renwick is a first-year engineering student pursuing a BSc. Electrical and Computer Engineering at The University of the West Indies, St. Augustine Campus, Trinidad and Tobago. In 2014, he was awarded a Fall internship at Prognostics Center of Excellence, NASA Ames Research Center. Under the mentor-ship of Dr. José Celaya and Dr. Chetan Kulkarni, Jason engaged in performing aging experiments of electrolytic capacitors. He returned in Spring 2015 for a second internship period during which he performed detailed analysis on the experimental data collected in his previous placement.

Chetan S. Kulkarni received the B.E. (Bachelor of Engineering) degree in Electronics and Electrical Engineering from University of Pune, India in 2002 and the M.S. and Ph.D. degrees in Electrical Engineering from Vanderbilt University, Nashville, TN, in 2009 and 2013, respectively. He was a Senior Project Engineer with Honeywell Automation India Limited (HAIL) from 2003 till April 2006. From May 2006 to August 2007 he was a Research Fellow at the Indian Institute of Technology (IIT) Bombay with the Department of Electrical Engineering. From Aug 2007 to Dec 2012, he was a Graduate Research Assistant with the Institute for Software Integrated Systems and Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN. Since Jan 2013 he has been a Staff Researcher with SGT Inc. at the Prognostics Center of Excellence, NASA Ames Research Center. His current research interests include physics-based modeling, model-based diagnosis and prognosis. Dr. Kulkarni is a member of the Prognostics and Health Management (PHM) Society, AIAA and Senior member IEEE.

José R. Celaya is a Senior Data Scientist at the Software Technology and Innovation Center, Schlumberger. Previously, he was the Lead Scientist and Co-lead at the Diagnostics and Prognostics Group and a founding member of the Prognostics Center of Excellence, both at the Intelligent Systems Division of NASA Ames Research Center. He received a Ph.D. degree in Decision Sciences and Engineering Systems in 2008, a M. E. degree in Operations Research and Statistics in 2008, a M. S. degree in Electrical Engineering in 2003, all from Rensselaer Polytechnic Institute, Troy New York; and a B. S. in Cybernetics Engineering in 2001 from CETYS University, México.

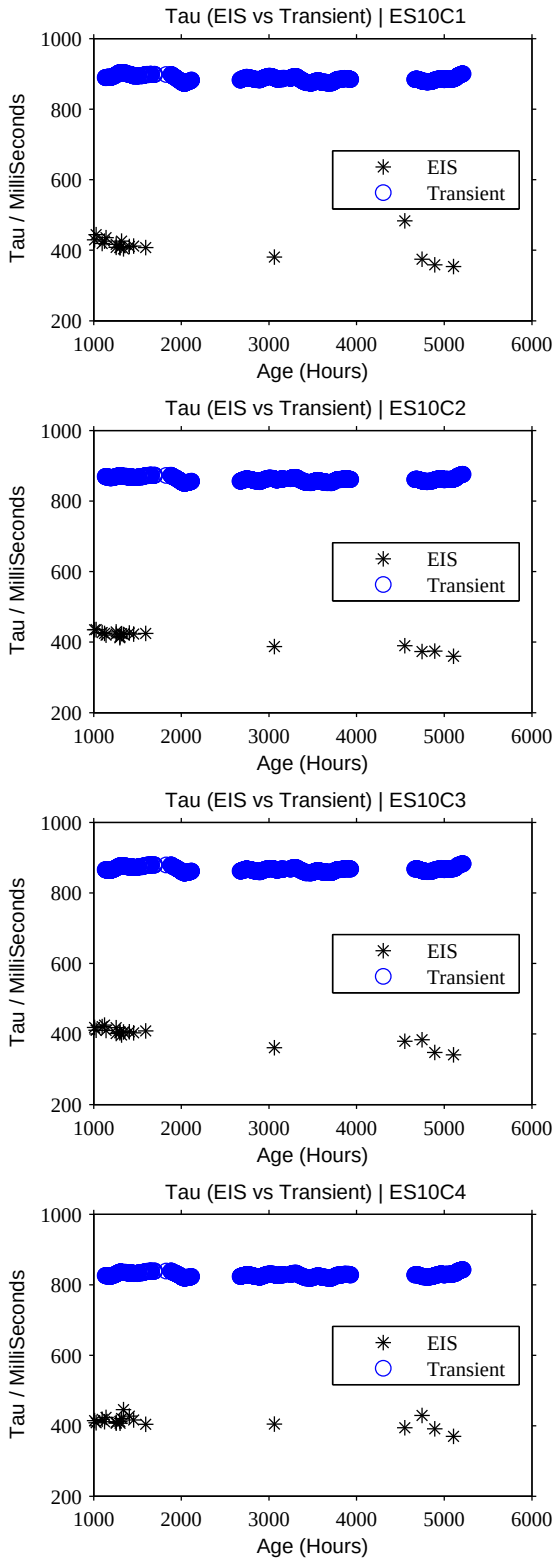

Figure 5. τ aging plots for all the devices under similar stress conditions(10V Board)

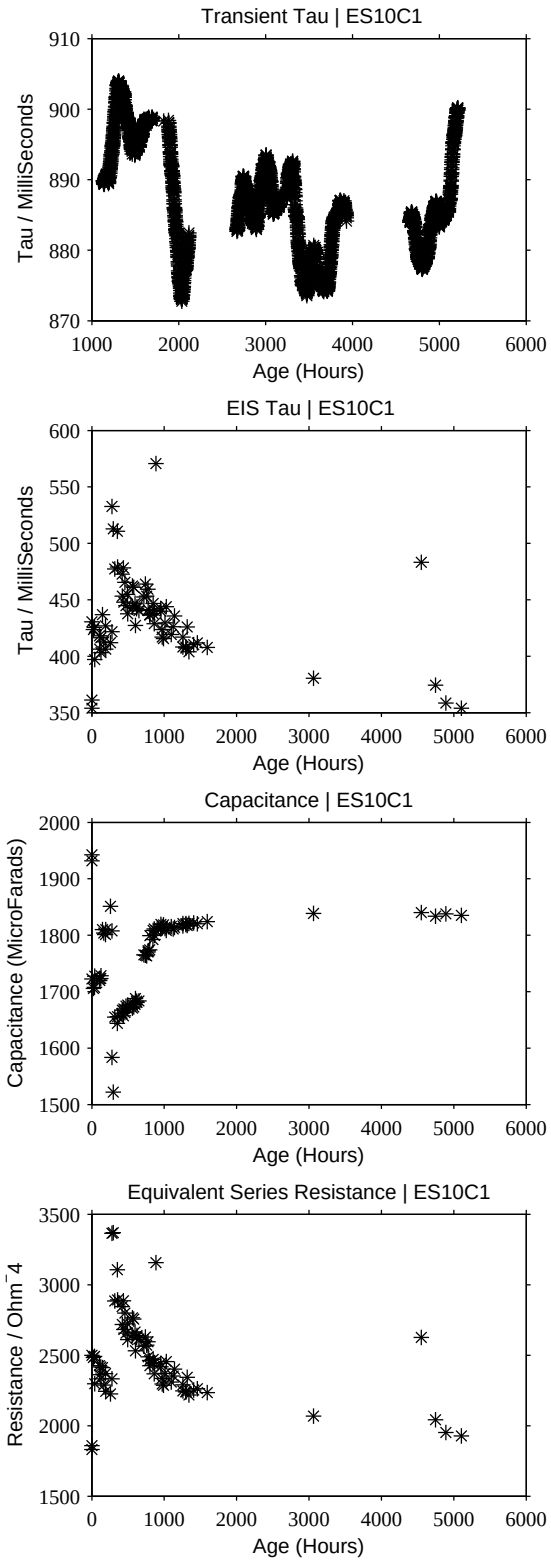

Figure 6. τ, C and ESR aging plots : Cap C5 (10V Board)