An Observer-based On-line Electrolytic Capacitor Health Monitoring System

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ABSTRACT

This work presents a cost-motivated method for reliability health monitoring of an electrolytic capacitor. The monitoring system uses a combination of analogue and digital electronics to optimize the cost. The capacitor aging is detected by on-line and in-situ detection of the evolution of the ESR (Equivalent Series Resistance) which is the most reliable ageing indicator. The algorithm uses waveforms naturally present in the power electronic train and thus the condition monitoring can be performed continuously and without interruption of the industrial process. The monitoring method estimates the ESR by adjusting a capacitor model that emulates the monitored capacitor. The limitation in accuracy of the estimation has no significant influence on the lifetime determination. The principle of the method is explained, along with the design tradeoffs and the monitoring procedure is described in detail. The paper also presents the experimental results obtained from a prototype during accelerated in-situ/inverter ageing tests.

1. INTRODUCTION

Electrolytic capacitors are amongst the most reported failures in power converters, heavily implying their overall reliability (Soliman, Wang & Blaabjerg, 2015). So detecting the ageing before the failure is essential to allow preventive maintenance.

The ageing of electrolytic capacitors is mainly due to the loss of electrolyte that slowly evaporates during operation, accelerated by operating temperature (Harada, Katsuki & Fujiwara, 1993). This occurs since the vapor passes through a rubber packing to limit the internal pressure. High level of ripple current is also responsible of internal self-heating and further accelerates ageing (Gasperi, 2005), (Kulkarni, Biswas, Koutsoukos, Celaya & Goebel, 2010).

Usage for a long period of time degrades also the electrolyte. For the industrial voltage-class capacitors, the best ageing indicator for electrolytic capacitor is the equivalent series resistance (ESR), while the equivalent capacitance remains rather constant. Much more variation is indeed expected from ESR since it is assumed to increase at least by +100% upon ageing, while at the same time the capacitance is likely to decrease by 20% (but usually less on this class of high voltage capacitors).

Many methods have been studied to determine ESR (Imam, Habetler, Harley & Divan, 2005), (Venet, Perisse, El-Husseini & Rojat, 2002), (Ertl, Edelmoser, Zach & Kolar, 2006). The accurate on-line ageing detection methods usually require either computationally intensive signal processing (Imam, Habetler, Harley & Divan, 2005) and relatively expensive hardware (powerful CPU, high sampling rate and accurate ADCs) or need complex (and potentially long-term variable) analogue processing (Venet, Perisse, El-Husseini & Rojat, 2002).

This paper presents an alternative solution for on-line monitoring (individual capacitor monitoring) based on a combination of simple analogue electronics and a low-end micro-controller. The functionality of the latter could be integrated in the DSP of the inverter at no additional cost. This enables an implementation for a mass production at low cost.

The ambitions of this paper are twofold: 1) show that while digital solutions are the most often investigated, an association of simple analogue pre-processing and very simple digital control can still give satisfying results; 2) show that of importance is the consistent performance over time, rather than absolute precision of ESR estimation.

This paper outline is as follows. First, the concept and the general architecture of the proposed method are presented. Then the detailed analysis and design rules are explained. Finally, some experimental results are presented and discussed.

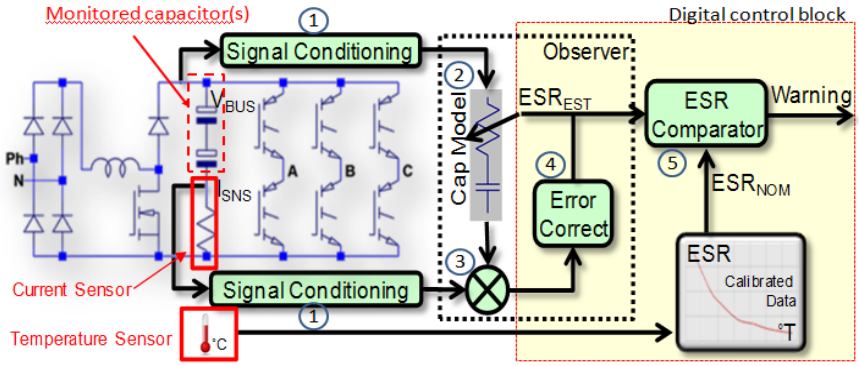

Figure 1. Functional diagram

Figure 2. Picture of the prototype.

2. MONITORING METHOD

The proposed method performs individual monitoring of a capacitor, using measurement of current flowing through the capacitor and voltage across it. The current is measured using a small value shunt resistor in series with monitored capacitor, though a non-invasive Rogowski-coil solution also exists. Figure 1 shows the block diagram of the proposed solution. Figure 2 is a picture of the prototype developed that embeds the capacitor(s) to monitor.

This board is connected to the DC bus of a power converter for operation.

Note that the internal ESR part of the monitored capacitor(s) is not represented on Fig. 1.

The monitoring method uses filtered capacitor voltage and current for operation. The filters allow the selection of ripple of interest, situated in the range of possible switching frequencies (where capacitor's impedance is dominated by ESR), which is similar to the proposed method in (Ertl, Edelmoser, Zach & Kolar, 2006). Since this parameter is highly temperature sensitive, a measurement of temperature is used to adjust the ageing limit accordingly.

Using an observer-based approach for ESR estimation permits flexible allocation of resource and complexity between the analogue and the digital worlds, resulting in a cost-optimal solution. The measured ripple voltage feeds an "adjustable capacitor model" which emulates the monitored capacitor in the frequency range of interest. This model generates an estimated ripple Iest which must match the measured ripple Imeas when the model is correctly adjusted, resulting in minimal difference between the two waveforms.

An estimation of ESR, ESR_{est} is thus obtained from adjustment of capacitor model.

With reference to Fig. 1, the analog part is composed of several blocks: (1) signal conditioning stages to filter and scale the voltage and current ripple; (2) the adjustable capacitor model, used to emulate the monitored capacitor; (3) a ripple comparison stage, which operates in time domain. The result of ripple comparison is then sent to the digital control block that executes the control algorithm (4) to adjust the capacitor model (tracking algorithm) and check for ageing (5) by measuring the increase of ESR_{est} with respect to healthy value.

The required digital control block is implemented either in a low-end micro-controller or possibly handled as an additional task in the main processor of the power converter, as the associated resources are minimal.

3. DETAILED ANALYSIS

In this section, we describe in more detail the different functions blocks together with the assumptions and design tradeoffs.

3.1. Current and voltage signal conditioning

The role of these signal conditioning blocks is to scale and filter the measured capacitor's voltage and current to extract the ripple of interest, in a region extending from several kHz up to about 80 kHz. A number of harmonics related to switching frequency are thus selected.

The filters attenuate strongly in particular the low frequencies considered as disturbances here (mostly harmonics due to front-end rectifier or electrical motor frequency and associated control loops). The needed band-pass filtering is composed of a combination of low pass (LPF) and high pass filters (HPF).

The scaling may be required to avoid saturation or to optimize the dynamic range of ripple depending on the application. An amplifier buffers the voltage developed across the shunt Rsh (current measurement). In our case a 10 mΩ, 1% resistor was used as a trade-off to optimize both

losses in resistor and avoid a too large amplification gain (to enable use of low cost operational amplifier). The frequency responses of both conditioning chains are almost identical (choice of 1% resistors and 5% class I capacitors is sufficient to satisfy this constraint).

3.2. Adjustable capacitor model

Functionally, once adjusted, the capacitor model delivers an estimation of ripple Iest which is supposed to be identical to Imeas, the measured current ripple.

The simple analogue capacitor model is composed of a fixed capacitor and a digitally adjustable potentiometer (digiPOT) to emulate the ESR part. The ESL part of capacitor is negligible at frequencies considered and is not emulated. The main assumption is that it is possible to emulate approximately the impedance of the monitored capacitor (with a scaling factor) at least in a frequency range where the impedance is dominated by the resistive part ESR. We are also taking advantage of the fact that the equivalent capacitance varies very little with age for this high-voltage class electrolytic capacitors.

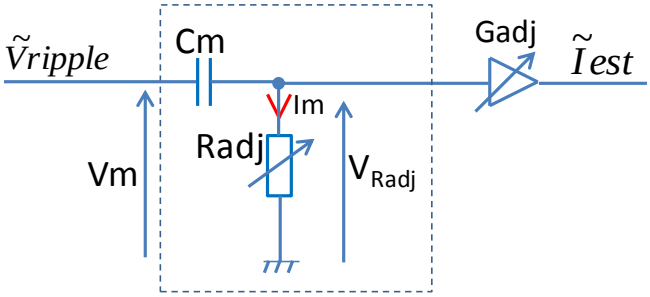

Figure 3.Capacitor model – principle.

The model delivers the estimated current ripple Iest, which is a scaled image of voltage across Radj resistor, proportional to model's current Im, as shown on Fig. 3.

The model's capacitor has a capacitance Cm which is a fixed scaled approximation of the monitored typical capacitance C. The basic design equation is Eq. (1) (equalization of time constants), considering the nominal values of components.

$$Radj \cdot Cm = (R_{sh} + ESR) \cdot C \quad (1)$$

The idea is to reproduce a capacitor model where capacitance Cm is much smaller than monitored capacitance C and a resistive part Radj much larger than ESR. The goal is to use a capacitance Cm in a range extending from 1nF up to 1uF, and a Radj in the range from one to 100 kΩ typically, to enable the use of a small capacitor and commonly available digiPOT.

Let's define a scaling factor K, such as:

$$Cm = \frac{C}{K} \quad (2)$$

$$Radj = K \cdot (R_{sh} + ESR) \quad (3)$$

The equation of the 256-tap adjustable potentiometer (neglecting its small Rwiper resistance) is as follows:

$$Radj = R_{\max} \cdot \frac{Cursor}{255} \Leftrightarrow Cursor = 250 \cdot \frac{Radj}{R_{\max}} \quad (4)$$

Cursor, comprised here between 1 and 255, allows the adjustment of the potentiometer. The adjustable potentiometer has its maximum value which corresponds to the maximum value of ESR at the lowest operating temperature, thus:

$$R_{\max} = ESR_{\max} \cdot K \quad (5)$$

where R_{max} is the full scale value of the adjustable potentiometer.

From Eq. (5), with ESR_{max}=1 Ω, we can choose K=10000 thus R_{max}=10 kΩ (full scale value of digitally adjustable potentiometer). With that choice, the estimated ESR resolution is approximately (1/255) ~ 4 mΩ.

From Eq. (2) : Cm=100 nF for C=1000 uF ➔ Cm can be a stable small ceramic class 1 capacitor (NP0 / C0G).

The resolution of the digiPOT is not critical for the application: a potentiometer with less steps can be used also (for instance 64 or 128), which simply limits the ability to detect small variations of ESR without consequence for the purpose of ageing detection.

The principle schematic Fig. 3 suggests that a variable gain amplifier Gadj should be used to measure and scale current that flows in the model (Im) to generate Iest. An optimized, simple schematic to implement the capacitor model is shown below (Fig. 4) that does not require a variable amplifier to scale Im.

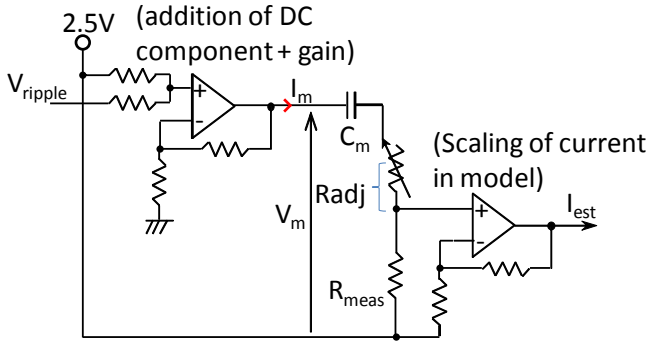

Figure 4. Capacitor model schematic.

A single digitally adjustable potentiometer is used for the "ESR" emulation part. An additional sense resistor R_{meas} is used to measure the current Im within the model. Of course R_{meas} determines the minimum value of ESR that can be emulated. A non-inverting amplifier then amplifies the voltage drop across R_{meas} with a fixed gain $G=K/R_{meas}$.

The value of the resistor R_{meas} is typically chosen small with respect to the full scale value of digiPOT Radj (10 kΩ). Also, since $Radj+R_{meas} \cong K.(Rsh+ESR)$, R_{meas} is conveniently chosen as:

$$R_{meas} = K \cdot Rsh \tag{6}$$

i.e. R_{meas}=100 Ω (with K=10000).

In that case, the minimum detectable ESR corresponds to the resolution of ESR_{est}. The required fixed gain to amplify voltage across R_{meas} is G=100, which limits the minimum "gain-bandwidth" product required for the operational amplifier used for the amplifier part (8 to 10 MHz is sufficient here).

Note that a first adder/buffer stage is used to impose the ripple voltage across the capacitor model composed of Cm in series with Radj and Rmeas. The addition of a DC component allows to use a low cost unipolar digitally adjustable potentiometer. The added DC component is removed at input of ripple comparison stage (AC coupling).

3.3. Ripple comparison

The current ripple extracted by filtering (Iripple) and current ripple estimated by the model (Iest) are compared in the time domain. A simple implementation of the ripple comparator, that compares only the positive parts of ripples, is illustrated on Fig.5.

The main comparator compares directly the instantaneous amplitudes of Iripple and Iest. The output of this comparator is applied to an averaging filter (LPF here) through a tri-state buffer. The filtered signal Comp_res evolves only when the tri-state buffer is enabled, which occurs when the other comparator detects that Iripple is superior to a small threshold Vth (to avoid comparison when signals are too small, i.e. when they carry no significant information).

Comp_res, once passed to the microcontroller, can be almost considered as a discrete signal (*) that behaves like a "trend" signal that indicates which of Iest or Iripple is higher on average.

The advantage of this approach is that there is no need to acquire at high sampling rate this low frequency trend signal, negating the need of employing fast high precision ADC as is the case for digital-only solution.

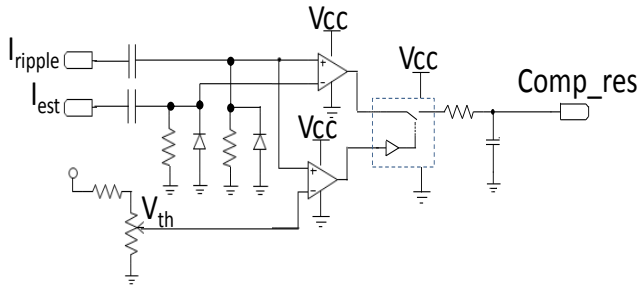

Figure 5. Ripple comparison.

(*) Remark: Comp_res is actually an analog low frequency signal with value between 0 and Vcc. It can be sampled at low sampling rate using an ADC (Analog to Digital Converter). But detecting that this value is above or below a threshold voltage (typically Vcc/2) is sufficient to determine the trend of comparison,

3.4. Tracking algorithm

The tracking algorithm employed to adjust the capacitor model operates by regularly incrementing or decrementing the value of the adjustable potentiometer depending on trend of ripple comparison signal Comp_res. Indeed, the trend signal Comp_res tends to increase when Radj is too high, and reciprocally to decrease when Radj is too low. The operation of the tracking algorithm is thus to adjust Radj so that Comp_res alternates around an equilibrium value (typically Vcc/2, i.e. "steady state" when on average 50% of the time one signal is higher than the other, considering that tri-state buffer is powered by Vcc).

If the evaluation period of the tracking algorithm is long enough (as in our case, every 1s) the signal Comp_res has time to evolve either towards 0V or Vcc (saturation output levels of the tri-state buffer) according to the trend of comparison.

Due to the discrete nature of digitally adjustable potentiometer, the ESR estimation oscillates between two adjacent values, determined by the ESR resolution which is approximately 4 mΩ. The software subsequently calculates the average of successive "cursor" values applied to

digitally adjustable potentiometer: $cursor_{avg}$. This value is then used to determine an estimation of ESR :

$$ESR_{est} = (\frac{Cursor_{avg} \cdot R_{\max}}{255} + Rmeas) \cdot \frac{1}{K} - Rsh \quad (7)$$

Which combined with Eq. (5) finally simplifies as:

$$ESR_{est} = \frac{Cursor_{avg}}{255} \cdot ESR_{\max} \quad (8)$$

(With ESR_{max}=1 Ω, R_{max}=10 kΩ, K=10000, Rsh=10 mΩ and Rmeas=100 Ω)

The estimated ESR_{est} value is not expected to be very accurate with respect to the "real" ESR of monitored capacitor. Indeed the absolute precision of this estimation depends on several parameters, in particular:

- Uncertainty on the fixed scaled approximation of C with Cm in the capacitor model (as explained in section 3.2): both C and Cm have their own tolerance on capacitance. C has a typical ±20% accuracy while Cm may be chosen with ±5% accuracy for instance:

$$\Rightarrow K(1-23{,}8\%) \le \frac{C}{Cm} \le K(1+26.3\%) \quad (9)$$

- The digiPOT maximum value has also a tolerance of ±20%: 8 kΩ <R_{max} <12 kΩ
- Some imperfections of analog processing paths may also slightly influence the estimation result (gain unbalance of estimation and measurement analog conditioning paths)
- Noise effect: susceptible of affecting the estimated and measured current ripples and thus also the accuracy of estimation by biasing the result of comparison. However, this is strongly alleviated by low pass filtering (or averaging) the successive values of estimated ESR (which is actually implemented in the prototype).

For the purposes of monitoring, most of the errors are removed when a self-calibration procedure (implemented in our prototype) is implemented in situ. The components of the monitoring system are chosen to have quite stable characteristics with time and temperature so that they do not significantly evolve during expected lifetime of the equipment. The compound error, after-self-calibration, of the monitoring system in estimating ESR evolutions is less than 5% for the entire temperature range and less than 1% at end-of life (Mollov, Foube, 2017).

3.5. Ageing detection

Ageing detection is performed by comparing current estimation of the ESR with an ageing limit defined for the current temperature. This ageing limit is typically defined by considering its allowed increase with respect to initial healthy value. Usually, a factor of two to three is considered, though a more meaning threshold is about 6 (Mollov, Foube, 2017). When the limit value is exceeded, an alarm is set to trigger a maintenance operation. Note that the initial "healthy" values are typically measured by the monitoring system itself during a self-calibration procedure executed during the early hours of operation. The calibration uses the same method to estimate ESR parameter and does not need specific operating mode of the power converter. This calibration method allows an accurate detection of increase of monitored parameter with ageing (since the initial value is not based on some typical, approximate value) and is another cost-control means.

4. VALIDATION / EXPERIMENTAL RESULTS

4.1. Test conditions

The monitoring system has been validated by connecting to the DC bus of a real power converter (TI Instaspin motor drive evaluation inverter) for realistic operating conditions. The load of inverter was composed of resistors and inductors to avoid the use of a rotating machine. The system has been checked at different operating points (up to 750W) but for convenience it was operated at ~100W output power for aging tests. To maintain a known operating temperature, and repeatable tests conditions, the monitored capacitor and the monitoring system were placed in a climatic chamber nearby the power converter. The ripple level within the monitored capacitor was quite low (about 200 mA_{rms}, well under its nominal rating: a few amperes). Self-heating of the capacitor is thus very limited, so that core and case temperature are expected to be almost the same. This facilitates comparison of on-line & off-line measurement at a given capacitor's temperature. For the high voltage class capacitors, the temperature at the terminals is a rather good approximation of the core temperature as the thermal impedance core-terminals is more than a magnitude smaller than that of the core-surface heat path. Thus we recommend placing the thermal probe for on-line monitoring with close thermal coupling to the capacitor terminals.

The case temperature was monitored using a thermocouple (not used in our monitoring algorithm) stuck on top of the monitored capacitor during these experiments. For off-line measurements, a sufficient time was given for stabilization (at least 20 mn) before each capacitor temperature measurement. During on-line operation, the difference between temperature measured respectively using the sensor of the prototype and the thermocouple were shown to be within ± 1°C once capacitor has reached thermal equilibrium.

The monitored electrolytic capacitor, studied from its healthy state until its aged state, was a typical type used for this kind of application: 1000uF, 400V. It was pre-

characterized in temperature and frequency during its early life to get reference data, using "off-line" measurement with an impedance analyzer. Figure 6 below shows the off-line measurements of ESR made initially (healthy capacitor) as function of frequency and temperature.

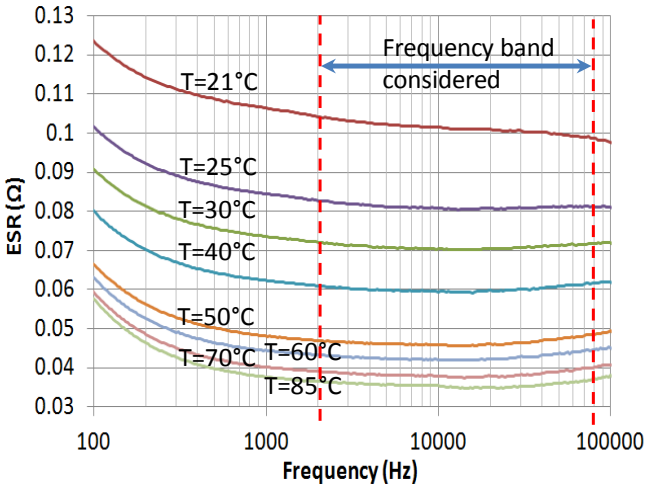

Figure 6. ESR vs frequency at different temperatures.

Note that we call "on-line" the estimation of ESR made with the proposed monitoring system. The capacitor under test and the monitoring system were placed in a temperature controlled oven for tests at T>Ta (ambient room temperature), while the inverter operates outside the oven.

During ageing test, the system has been stopped regularly to perform on-line measurements at different temperatures. Also an off-line measurement (at ambient temperature) was done in order to detect when end of life is reached. The goal was to assess the ability of the monitoring system to detect the ageing state.

4.2. Results & discussion

Figure 7 summarizes a few results obtained at the beginning of life of capacitor (healthy state). The "off-line" curve is the pre-characterization of monitored capacitor, ESR function of temperature and frequency. Since ESR is not absolutely constant in the band of frequency considered (see Fig. 6), an average value of ESR over this interval is considered to determine the off-line ESR value.

As can be seen, the off-line curve is quite close from on-line measurement: measured accuracy is within ± 10% on this prototype.

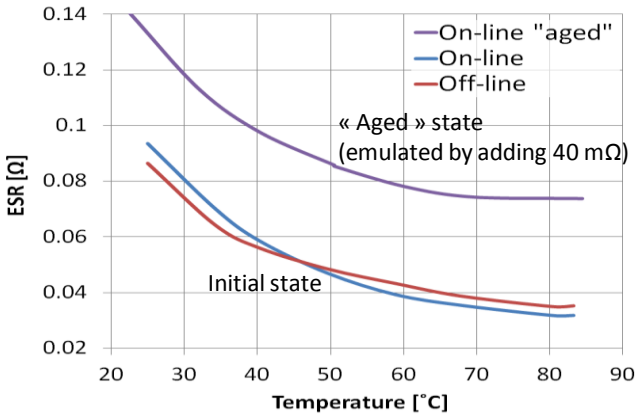

Figure 7. On-line measurements (healthy & simulated ageing).

More interesting is the on-line "aged" curve, where an additional resistor of 40 mΩ was connected in series with monitored capacitor to emulate an ageing: it shows that this curve is really close to a simple translation of healthy capacitor curve.

Current result of natural ageing tests and comparison with off-line measurement (at ambient lab temperature) is presented on Fig. 8. The relative increase of each curve is calculated with respect to the initial value, measured in healthy state.

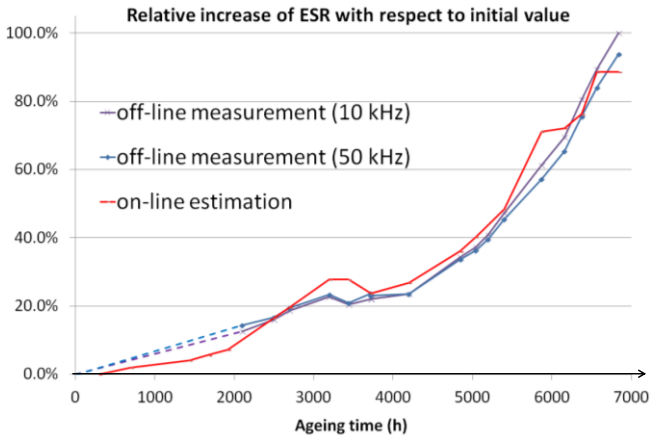

Figure 8. Comparison between on-line & off-line measurement.

The graph shows the small difference between two off-line ESR curves measured respectively at 10 and 50 kHz. The ESR "measured" by the on-line monitoring system is expected to be proportional to off-line measurement in this band of frequency since it contains the most significant harmonics on our experiment (SVPWM modulation, with switching frequency Fsw=10 kHz).

The red curve is the on-line measurement. The on-line measurement and off-line measurement match quite well. Some fluctuations are due to operation at slightly different room temperatures: ESR varies a lot in the interval 21°C ... 23°C.

From 0 to about 4200h, the ageing has been made at 85°C which is the rated temperature for the selected capacitor. Starting from 4200h, the ageing has been slightly accelerated by increasing the oven's temperature to 105°C. This explains the acceleration of the degradation of the capacitor. Still, the ageing has taken a long time because the capacitor was operated at low ripple level: the temperature is the only real stressor here.

Figure 9 shows a comparison of on-line and off-line measurements at beginning and end-of–life. Note that here we use the classical criterion of "double the ESR value at room temperature" for end-of-life.

The off-line measurements were made under the same conditions at beginning of experiments (healthy state) and after ageing (almost 7000h), by connecting a cable directly between the capacitors terminals and the impedance analyzer. The cable impedance was compensated for the measurement. Also, the prototype has not been modified during this ageing period.

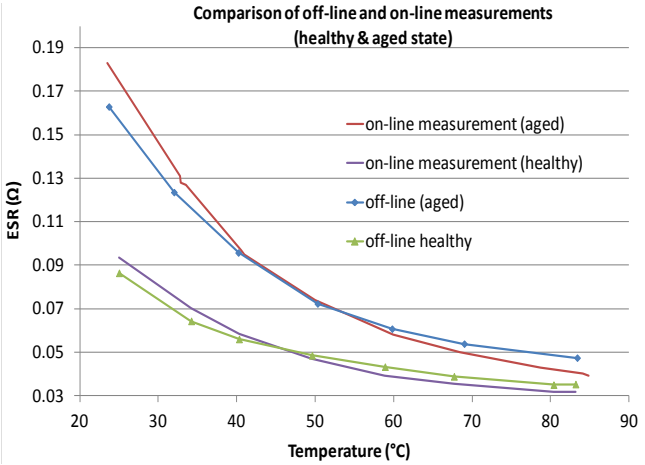

Figure 9. Comparison of on-line & on-line measurements (healthy & aged state).

As can be seen, the behaviour of the estimated ESR obtained with monitoring system is similar at end of life and in early hours of operation: values are slightly overestimated in the low temperature range up to 45°C. Above that temperature, the results appear under-estimated with respect to off-line measurements.

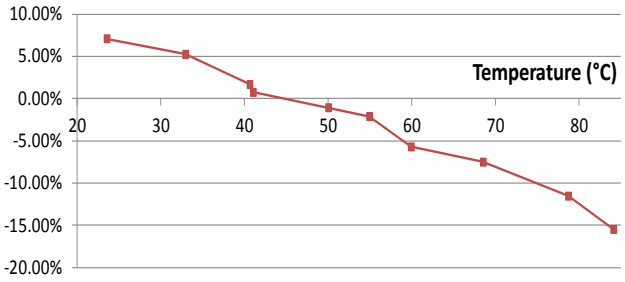

Figure 10. Difference between on-line & off-line measurement (aged state).

The normalised difference between on-line measurement and the off-line measurement is shown in Fig. 10. On this prototype it is within ± 10% up to about 75°C, which is quite comparable to results achieved at beginning of life. Some of the differences between on-line and off-line measurement is attributed to the more complex waveforms used for on-line estimation compared to a purely sinusoidal excitation used on the off-line measurement. Both measurements types remain consistent and repeatable over the age of the capacitor.

The following graph (Fig. 11) shows the ratio of ESR_{est} in aged and healthy state, compared to the ratio of ESR measured off-line in the same conditions.

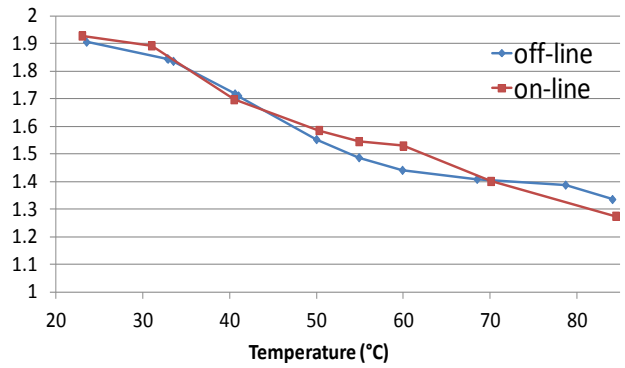

Figure 11. Ratio $ESR_{aged}/ESR_{healthy}$ (on-line & off-line).

We see that the ratio of $ESRest_{aged}/ESRest_{healthy}$ is very close to $ESR_{aged}/ESR_{healthy}$. This confirms the ability of the system to detect quite accurately the increase of ESR.

5. CONCLUSION

This paper presents a low-cost and on-line method to reliably detect ageing of an electrolytic capacitor.

The method was implemented and validated in a prototype. Measurement is performed during normal operation of the

power converter over a large range of operating points, and does not require knowledge or presetting of the converter operating point.

Despite a compromise on absolute accuracy of the ESR estimation, it is able to detect reliably (with repeatable results and an accuracy within 10%) the increase of the ESR of a capacitor upon ageing, with respect to the measured initial value.

This method would be applicable to monitor capacitors on any converter with a DC bus as long as it presents enough switching ripple to allow operation.

A perspective for future work is to use the history of collected data (evolution of ESR, operating temperatures) to extrapolate the remaining useful life of monitored capacitor in order to plan the replacement of the capacitive bank.

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