Symbolic Dynamics and Analysis of Time Series Data for Diagnostics of a dc-dc Forward Converter

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ABSTRACT

This paper presents a novel approach to diagnosis of dc-dc converters with application to prognosis. The methodology is based on Symbolic Dynamics and Diagnostics. The data derived method builds a statistical baseline of the converter that is used to compare future statistical models of the converter as it degrades. Methods to determine the partitioning and number of partitions for the Symbolic Dynamics algorithm are discussed. In addition, a failure analysis is performed on a dc-dc forward converter to identify components with a high probability of failure. These components are then chosen to be monitored during accelerated testing of the dc-dc forward converter. The methodology is experimentally validated with data recorded from two dc-dc converters under accelerated life testing.*

1. INTRODUCTION

Diagnostics methodologies attempt to determine the current state of health of a system and flag any type of anomalous behavior that could affect the operation of the system. Successful diagnostics can eventually lead to prognostication of a system where prognostication is the prediction of the remaining useful life of the system under monitor (Hess et al., 2005)

The goal of diagnostics and health management in general is to maintain system operability, reduce maintenance costs, and maximize safety. Diagnostics and health management of electronic systems can be obtained by numerous different methodologies. Most of these can be sorted into either a data driven or model based category. Model based methods, such as the name implies, rely on a physical model representation of the system and the underlying degradation process (Brown et al., 2006). On the other hand, data driven models tend to model the degradation of a system by long term monitoring of the system. This methodology tends to require large data sets in order to train the data driven models used to generate the health measures.

In this paper, we aim to develop a methodology based on Symbolic Dynamics (SD) (Ray, 2004; Rohan, 2006) that can be used to generate diagnostic measures from a degrading dc-dc converter. Symbolic Dynamics has been applied to many systems including inverter fed induction machines (Rohan et al., 2006), fatigue crack diagnosis (Singh et al., 2010), and in nuclear power plant operations (Jin et al., 2011).

In this paper, we used a dc-dc forward converter for our test subject. Data is recorded from an accelerated test of these converters on an hourly basis and is used in the algorithm. It is our intention to expand the results into a prognostic algorithm that can deduce the remaining life of the converter from the current anomaly generated by the SD algorithm.

Symbolic dynamics lends itself well to the area of electronic diagnostics as it is a relatively simple algorithm to implement. In general, the algorithm analyzes the data captures and forms states based on the data. These states are then tracked statistically through time. These states can be designated in numerous ways; that is, the states could directly be related to the data points themselves or represent the duty cycle of the converter.

This paper is organized as follows. Section 2 presents a background on the Symbolic Diagnostics and Analysis methodology. Section 3 focuses on the dc-dc converter and the accelerated testing of the converter to generate the experimental data used in the algorithm. Section 4 presents the results of the algorithm compared to other electronic system diagnostic metrics. Finally the paper concludes with a short conclusion and future work suggestions.

2. SYMBOLIC DIAGNOSTICS AND ANALYSIS OF TIME SERIES DATA

Diagnostics of the converter is accomplished through the use of symbolic diagnostics and analysis of time series data (Ray, 2004). In this work, we propose a methodology to accomplish diagnostics of a dc-dc converter in real-time with the use of this tool. The method depends on symbolizing the captured time series data, generating states that consists of permutations of generated symbols, and calculating the probability of these states.

In general, the probability of the states change as the converter ages and degrades. Tracking these changes allows for quantification of the degradation in the dc-dc converter over time. These changes can be quantified by comparing the current analysis to a baseline case. Two underlying assumptions must be satisfied in order to use symbolic dynamics. They are:

1) The system degradation mechanisms must be dynamically separate from the system dynamics; and
2) The system generates monotonically positive anomaly measures.

The first requirement is a two time scale separation argument. If the system dynamics are much faster than the degradation mechanisms, then individual data captures will contain stationary degradation dynamics. The second assumption states that the system does not exhibit self-healing or is repaired. This assumption is flexible in that a non-monotonically increasing anomaly can make diagnosis more difficult but not impossible. A monotonically positive increasing anomaly also pushed the methodology towards a prognostics tool.

The dc-dc converter satisfies assumption one as the system dynamics are monitored through time. The dynamics of the dc-dc converter are based on the switching frequency of the converter, that is, 100 kHz. A short data capture is taken at a faster rate than the switching frequency and is used to determine the current system state of health. During this short interval, the degradation in the converter can be considered stationary. For assumption two, the converter is allowed to age without repair. The degradation in the converter continually increases and with the anomaly quantification metrics, generates an increasing anomaly measure.

The methodology for Symbolic Dynamics begins by first determining the number of symbols to use in the definition of the symbolic sequence and also defining the partitions to assign symbols to time series data points which is closely related to defining the number of symbols. Each data point is assigned to a unique symbol. This step can be considered as a coarse quantization of the time series data.

With the symbolic series now generated, the next step is in determination of states for the algorithm. States are simply defined as groupings of *D* symbols. Throughout this paper, the choice *D*, called depth in the algorithm, is chosen to be unity; that is, each symbol results in a state. Once the states are defined, the probabilities of occurrence of the states are used to generate an anomaly in the behavior of the system that is related to degradation. Currently, there are numerous metrics to quantify an anomaly based on these state probabilities.

The algorithm will now be discussed in more detail including the partitioning of the time series data, generation of the symbolic sequence, and the determination of parameters in the algorithm. With the completion of symbolization, the discussion will continue with defining an anomaly based on the statistical model generated from the time series data.

2.1 Choice of Number of Symbols

In order to enable the partitioning of the time series data, the choice of the number of symbols in the algorithm must be determined. Two methods are presented, one for each type of partitioning methodology. The partitioning methods will be discussed in the next section. Each method is based on the entropy of the resultant symbol distributions generated from the partitioning method.

For uniform partitioning, the choice of number of symbols to use is defined by the use of Entropy Efficiency. Entropy Efficiency is given as:

$$E_e = \frac{\sum_{i=1}^{N} p_i log_2(p_i)}{log_2(N)} \quad (1)$$

where p_i is the probability of the ith symbol. The $p_i's$ are calculated at each iteration of the search for *N* and represent the probability of each individual partition. The logarithm is taken to the base 2 such that result of entropy is based in bits. The aim is to determine the maximum of Eq. (1) over uniform partition size, *N*.

Equation (1) can be interpreted in two ways. First, the denominator term acts as a penalty term for larger distributions that is a large choice of *N*. This enforces computationally a more efficient algorithm.

Secondly, this metric measures the entropy deviation from the ideal entropy given by a uniform distribution (represented in the denominator term). For source distributions that are not known a priori, a good estimate for the source distribution is that from a uniform probability if there are no constraints or assumptions on the underlying generating symbol distribution (Conrad, 2011).

An issue associated with this method that must be kept in mind is if during the process of looking for an optimal number of states is if a state is generated that has a null symbol occurrence probability. This would cause the entropy estimate to be undefined. In this case, the search concludes with the generation of the first null symbol probability.

For ME partitioning, we again turn the use of entropy under a method developed by (Rajagopalan & Ray 2006). This method estimates the number of states through the use of histograms. To estimate the number of states we use the differential entropy of the time series data given as:

$$h(x) = -\int_{-\infty}^{\infty} p(x) log_2\big(p(x)\big)\, dx \qquad (2)$$

where x is the possible values the data can take and $p(x)$ is the probability density of x. Once the entropy for the time series data is estimated, the number of symbols for ME partitioning is given by:

$$N = argmin_k\{log_2(k) - h(x) \geq 0\} \qquad (3)$$

that is, we obtain a distribution whose entropy is greater than or equal to that of the entropy estimate from the time series data. The number of symbols N is chosen to be the minimum k that satisfies Eq. (3).

A difficulty with differential entropy is the ability of this measure to take on a negative value. If this is the case, the algorithm defaults to a selection of two for the number of symbols.

2.2 Partitioning

After the number of partitions has been determined, the next step of the algorithm requires symbolization of the time series data. This step includes the determination of the partitioning structure of the time series data used in the generation of the symbol sequence. This step requires the number of symbols used in the algorithm as well as the partitioning methodology of which includes uniform and Maximum Entropy (ME) partitioning to be determined. The choice of the number of symbols will fix the number of partitions in the algorithm as each partition is assigned a unique symbol as was discussed previously.

The objective of the partitioning is to assign a symbol to each of the time series data points $X \equiv (x_0, x_1, \cdots, x_n)$. Given the set of N symbols, $\sum = (s_0, s_1, \cdots, s_{N-1})$, each symbol s_i is assigned to one partition P_i, where P is the partitioning of the time series data $P \equiv (P_0, P_1, \cdots, P_{N-1})$. Therefore, if $x_i \in P_i, x_i \rightarrow s_i$, that is, we assign s_i to x_i if x_i falls within the bounds of P_i. As mentioned earlier, there are two methods to develop the partitioning P and they are called uniform partitioning and ME partitioning.

Uniform partitioning requires taking the range of the time series data and dividing it into the N mutually–exclusive equally spaced partitions. Each time series data point that falls into one of these N regions is thus assigned a unique symbol.

The other popular method for time series data partitioning is by Maximum Entropy. This partitioning scheme, as hinted by its name, is completed by maximizing the entropy of the resultant symbol occurrence probability. That is, the occurrence probability of the symbols should be uniform in nature.

In order to complete this, the time series data is ordered in magnitude. By grouping the ordered data into subgroups of length X/N, the partitioning structure for ME partitioning is defined. The resultant occurrence probability for these partitions in the baseline case becomes equal. This differs from the results of uniform partitioning as the resultant probabilities are generally not uniform.

In theory, the total number of partitions can range from a simple binary partition to an upper limit defined by the total number of unique samples in X. In the former case, each data point is simply relabeled with a unique symbol.

2.3 Anomaly Generation

With the completion of the partitioning and symbolization, it is left to determine how to quantify an anomaly from changes in the underlying statistical behavior of the system. The deviations in the system are captured through changes in the state occurrence probabilities. In the case of unity depth, D is equal to one, the states that are tracked during life testing are simply the symbol occurrences. In general, if D is not unity, the states of the system consist of permutations of groups of D symbols. In the following, the states are thus the symbol occurrence probabilities as D is set to unity.

In this work, two measures are used to quantify this change and define it as an anomaly A. One is based on a Euclidean distance type measure and the second is based on the Kullback-Leibler divergence (Singh et al., 2010). Both of these measures use the baseline distribution of state probabilities as well as the current distribution to generate an anomaly.

The Euclidean measure is the 2-norm difference between the baseline and current system state probability

distributions. Given the state probability vector p, the Euclidean metric is:

$$A = \|(p_{nominal} - p_i)\|_2 \quad (4)$$

where $p_{nominal}$ is the baseline state probability vector and p_i is the current state probability vector. The baseline SPV is based on the healthy condition of the system such as at the start of use. The other measure implemented in generating an anomaly from the statistical models of the system is the Kullback-Liblier divergence:

$$KL = \sum_{i=1}^{N} p_i^k log\left(\frac{p_i^k}{p_i^{nominal}}\right) \quad (5)$$

In (5), the sum is over the total N states in the algorithm while k represents the k^{th} iteration of the algorithm. An anomaly measure is generated from (5) by:

$$A = 0.5\left(KL(p^k, p^{nominal}) + KL(p^{nominal}, p^k)\right) \quad (6)$$

These anomalies are then used to diagnose the current state of the converter as the system degrades from use. From these measures, it is possible to detect degradation or a fault that has occurred in the system.

3. ACCELERATED TESTING OF A DC-DC FORWARD CONVERTER

In order to verify the algorithm, a 50W forward converter was designed, constructed, and placed in an accelerated life test environment. The forward converter used 15 V for input and output 10 V at 5 A nominally. The general circuit diagram of a forward converter is shown in Figure 1 with the locations of the sensors implemented in the testing. This converter implements the current-mode feedback methodology in addition to output voltage feedback.

It is known that specific components in the dc-dc forward converter are more susceptible to failure than other components. From (Orsagh et al., 2006; Orsagh et al., 2005), the most probable locations of failure for the converter are the MOSFET power switch, the rectifying diodes, and the input and output capacitors.

The accelerated test consisted of placing the converter in an oven to generate a High Temperature Operating Life (HTOL) test. This test is geared to ascertain the usable life of a system by continually running the system at high environmental temperatures. In this case, the converters were continually run at 85°C. This temperature point coincides with the maximum operating temperature of several components in the converter. These components included the Pulse-Width-Modulator (PWM) controller, input/output electrolytic capacitors, and several other integrated circuits.

The high temperature was used to accelerate failures in the dc-dc converter. For example, the electrolytic capacitors contained in the circuit would be directly affected by operating temperature. The higher temperature would cause acceleration in the loss of electrolyte in the capacitor causing wear out (Kulkarni et al., 2009). This in turn would cause an increase in the capacitors equivalent series resistance (ESR).

Additionally, the power MOSFET failure mechanism of Time Dependent Dielectric Breakdown (TDDB) can be accelerated by higher temperatures (Kalgren et al., 2007).

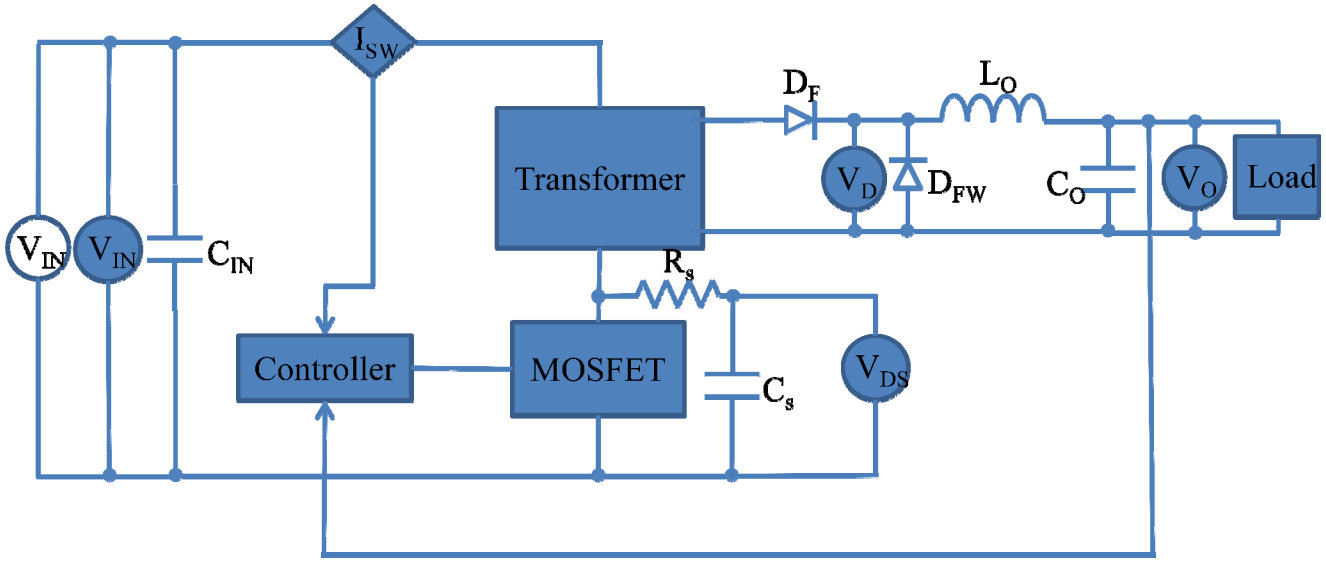

Figure 1: Simplified Diagram of a dc-dc Forward Converter with Sensor Locations

Another failure phenomenon that can be accelerated with higher temperatures is electromigration affecting both MOSFETs and rectifying diodes. These two components are also susceptible to degradation caused by interdiffusion.

3.1 Sensor Placement

Although each component will degrade individually and sensors have been placed at these components to observe degradation, the objective of this research is not to specifically identify the failure mode of a specific component. Instead, the objective is to capture data across locations in the converter that have high probability of degradation and/or failure to generate a diagnostic measure for the system as a whole.

Sensors were placed in the circuit that would maximize the probability of observing degradation in the components mentioned above. In addition, the input voltage was also monitored throughout the testing.

Voltage sensors were placed across the power MOSFET, the freewheeling diode (D_{FW}), and at the output voltage, V_O. In addition, the current signal produced from the current sensor for current-mode feedback was also used in the degradation monitoring. Since this signal was already being monitored for current mode control, it provided an easy means to access the instantaneous switch current waveform.

Thermocouples were placed on the tabs of the TO-220 package for the MOSFET and diode D_{FW} for monitoring as well. During each time series data capture, one sample each was taken of the MOSFET, D_{FW}, ambient, and oven temperatures for monitoring during testing.

Data for the SD algorithm was recorded from these sources at a rate of 800 KS/s. The data acquisition hardware was triggered every hour to record a data snapshot of 0.25s in duration. No anti-aliasing filters were implemented in the data acquisition hardware. The data channels were buffered into NI 9221 analog input modules.

Anti-aliasing filters were not implemented as the filtering function could remove degradation information from the signals. Since the sampling rate is approximately eight times the switching frequency of the converter, the anti-aliasing filters would have filtered too much of the frequency spectrum of the signals. The anti-aliasing filters would remove significant energy from the spectral content of the time series data. Given that our objective is to not recreate the time series date, it is acceptable to have a limited sample rate on large bandwidth signals. More research is currently being performed on the affects of the low rate sampling on the performance of the symbolic dynamics algorithm.

3.2 Life Testing

The forward dc-dc converter was placed into the temperature chamber and allowed to function until failure of the converter. Failure was defined as failure to maintain desired output voltage within 10% of the set point or as the result of complete failure.

For testing, the converter was loaded with a bank of 0.5 Ω resistors used to create a 1 Ω load for the converter. The voltage output of the converter was set at 9.5 V across the 1 Ω load. This resulted in a continuous output power of about 90 W. The converter would then be continually loaded at this power level while under the HTOL testing. Further research will investigate the effects of changing load on the results of the methodology.

The converter had a 24 hour burn in procedure to confirm functionality of the converter and data acquisition systems. This period also allowed the system to reach an operational steady state before the stress testing began. The temperature of the oven during burn in was 65°C. After this period of time, the accelerated testing was started. The temperature of the oven was increased to 85°C at this time. This temperature was selected due to the operational temperature constraints of the onboard electrolytic capacitors and integrated circuits (ICs).

The first converter was operated for 200 hours after the burn in period was completed. At this time, the converter failed by not being able to maintain the desired output voltage. Post failure analysis pointed to the input capacitors as the failed components. Table 1 shows the pre and post test conditions of all electrolytic capacitors in the converter which demonstrate the degradation experienced by the capacitors

	Pre-Test		Post-Test	
Capacitor	C (µF)	DF	C (µF)	DF
C1	455	0.049	415	0.487
C2	449	0.05	241	1.24
C3	449	0.047	128	1.96
C4	204	0.057	200	0.057
C5	204	0.058	199	0.058

Table 1: Capacitor Characterization for Converter Test 1

In the table, C1-C3 were the input capacitors (C_{IN} in Figure 1), C4 was the output voltage capacitor (C_O), and C5 was used as a filter for a negative voltage bus in the converter (not shown in Figure 1). DF in the table is the Dissipation Factor of the capacitors and is related to the loss tangent for dielectrics. The higher the DF value results in a larger magnitude of the ESR component of the electrolytic

capacitor generating higher internal power losses in the capacitor. The relationship between DF and ESR is:

$$DF = \frac{ESR}{|X_C|} \quad (7)$$

where X_C is the reactance of the capacitor under the test at the known test frequency.

As is visible in the table, capacitors C2 and C3 suffered severe damage from the testing. This is representative in both the reduction of the capacitance (nominally 470 µF) and the increase in the DF measure of both capacitors. Confirmation of the failure was completed by restoring the converter to normal functionality by replacement of these capacitors (C1 though C3). Replacement of these capacitors restored the output voltage capability of the converter.

Similarly, a second test was carried out under the same test conditions for failure repeatability with a new converter. This test lasted approximately 1,800 hours at the 85°C test at which point the test temperature was increased by 10°C in order to accelerate the test. At this temperature point, the converter functioned for another 152 hours.

After failure, it was determined that the failure was again the input capacitors of the converter. Table 2 shows the capacitor characterizations before and after the testing.

	Pre-Test		Post-Test	
Capacitor	C (µF)	DF	C (µF)	DF
C1	434	0.043	377	0.617
C2	434	0.043	371	0.694
C3	427	0.045	363	0.800
C4	203	0.051	194	0.087
C5	203	0.052	143	0.53

Table 2: Capacitor Characterization for Converter Test 2

Test 1 and test 2 capacitors showed some signs of the top of the canisters bulging. This is most likely related to loss of electrolyte through evaporation due to internally generated heat in the capacitor.

The difference in test lengths is most likely due to component differences in the converters such as those from different lots. The capacitors used in the converters were from the same manufacturer but not from the same production lot. The tables also demonstrate the amount of degradation the capacitors incurred during testing specifically in terms of the dissipation factor. In terms of the data derived method, the difference in test lengths will not negatively affect the performance of the algorithm as will be seen in the upcoming sections.

The other components observed during testing (MOSFET and rectifying diodes) did not show significant changes in parameters after testing. Parameters tested for the MOSFET included $V_{GS,th}$, the gate threshold voltage, approximate $R_{ds,on}$, gate leakage current, and BV_{DSS}, the maximum drain to source voltage. The rectifying diode parameters included V_{FW}, the forward voltage, and the maximum cathode-anode voltage. All of the above parameters recorded minimal changes from pre to post-testing.

4. RESULTS

Once the data collection was completed with the failure of the converters, the SD algorithm was implemented on the captured data sets. The goal of the algorithm is to generate anomalies using the collected data that can be used to determine the state of health of the converter.

The SD algorithm results are compared to features that are commonly used to monitor the health of electronics. The estimated efficiency of an electronic system has been used to determine the current state of health of the system as a loss of efficiency is a sign of system degradation (Orsagh et al., 2005). Efficiency can be monitored through implementation of sensors on the input and output ports of the system to monitor current and voltage. As the components in the system begin to degrade, they tend to have more internal power loss that directly affects the converter's overall efficiency. This degradation can be tracked through the computation of the system's efficiency.

When the testing of the converters was first started, it was not anticipated that an efficiency measure would need to be calculated so input and output currents were not measured. However, input and output voltage was measured and switch current was also monitored. From these three variables plus knowledge of the load enabled efficiency to be estimated from the captured converter signals.

From the captured data, the input current had to be estimated from the captured switch current. This required the duty cycle to be estimated from the data captured from the converter. Once the duty cycle was estimated, the current was scaled by the duty cycle and the mean taken from current data when the switch is ON. This was calculated as:

$$I_{in} = mean\left(i_{sw,ON} * D\right) \quad (8)$$

where $i_{sw,ON}$, is the switch current during the ON interval and D is the duty cycle.

Another feature to be compared to the SD algorithm is related to the output voltage ripple of the converter. As the output capacitor degrades, the ESR of the capacitor tends to

increase causing more output voltage ripple. To attempt to capture this effect, a form factor metric given as:

$$F_F = \frac{V_{O,RMS}}{V_{O,MEAN}} \quad (9)$$

was implemented to track the output ripple characteristics.

Symbolic dynamics was applied to the time series data recorded from the accelerated testing of the converters. Since there was uncertainty in which signals would produce the best results, the algorithm was implemented on all signals using the automatic selection methods discussed in Section 2.2.

From the results of the algorithm implementation, it was discovered that the signals containing the best degradation trending was the diode voltage (DFW in Figure 1). An example of the diode voltage is shown in Figure 2. This data was taken from the first converter test.

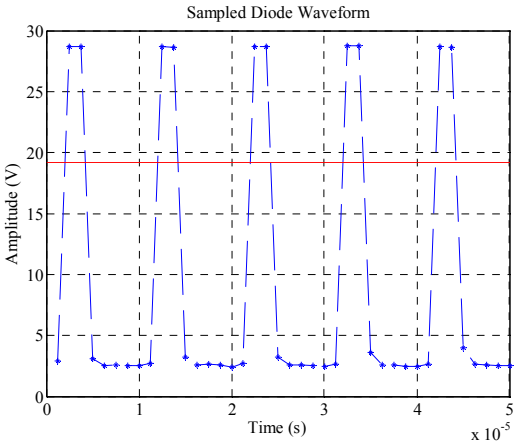

Figure 2: Sample Diode Data with Partitioning (Red) - Healthy

As seen in the figure, the data is sampled at 800 kHz resulting in eight data points per cycle in the waveforms. The binary partitioning implemented in this analysis generates an interesting result. The upper partition probability of occurrence is the duty cycle of the converter. In this case, the algorithm automatically defaults into a duty cycle detector and tracker.

The diode's voltage works well as the wave shape of the voltage is a pulse waveform in nature. The pulse wave shape enables a direct correlation of duty cycle of the converter to the converter's current operating condition. The duty cycle of the converter is a good feature to use for converter health. As the converter degrades, in order to maintain the current output power, the duty cycle must be perturbed slightly larger. The duty cycle needs to increase because as the converter degrades the efficiency of the converter also decreases as internal components begin to become more lossy. The efficiency of test 1 over the complete interval is seen in Figure 3.

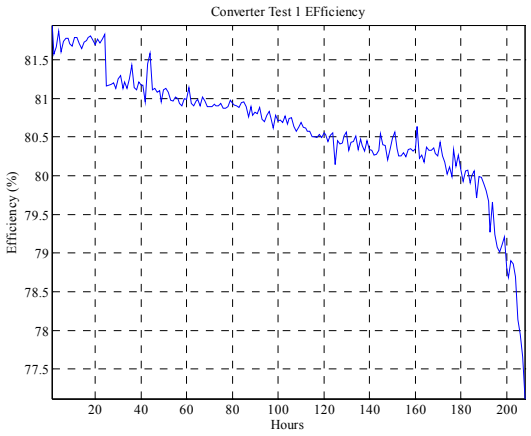

Figure 3: Test 1 Efficiency over Accelerated Testing

The efficiency of the converter decreases throughout the accelerated converter testing. To overcome the additional losses in the converter, the closed loop control perturbs the duty cycle to maintain output power. The duty cycle for test 1 is shown in Figure 4.

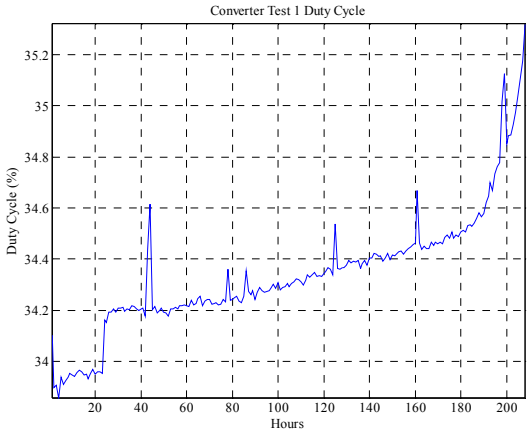

Figure 4: Converter Test 1 Duty Cycle over Accelerated Testing

As the testing progresses, the increasing degradation in the system causes the duty cycle to be increasingly perturbed. From the plot, the converter started at approximately 34% and failed when the duty cycle reached just over 35%.

Figure 5 shows the captured diode data after 200 hours of degradation also from the first test.

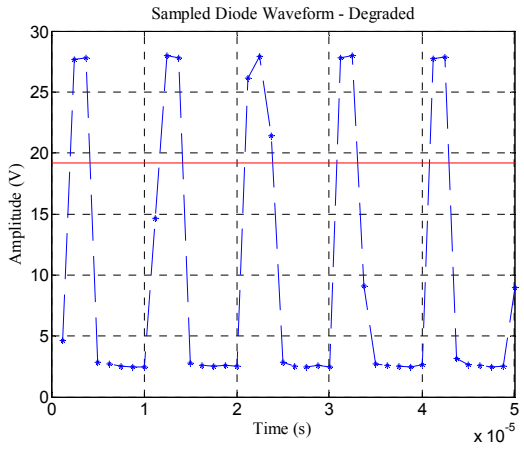

Figure 5: Sample Diode Data with Partitioning (Red) – Degraded

In Figure 5, note that the same partition is used in the example. The partitioning must remain invariant across the lifetime of the system for proper operation. Also note that due to the degradation, there is an additional data point in the upper partition. This in turn increases the upper partition's occurrence probability which can be interpreted as an increase in the duty cycle of the converter.

4.1 First Converter Test

The results in Figure 6 are from the captured diode data using the binary partitions shown in Figure 2 and 5. The anomaly was generated from the state probability vector where the states are the partitions themselves (depth was set to 1). The anomaly metric used in the figure was from (4). The baselines used in all the cases were from the initial start of the burn in. It is possible to use any point in the test for the baseline. In this case it was convenient to use the first set of captured data.

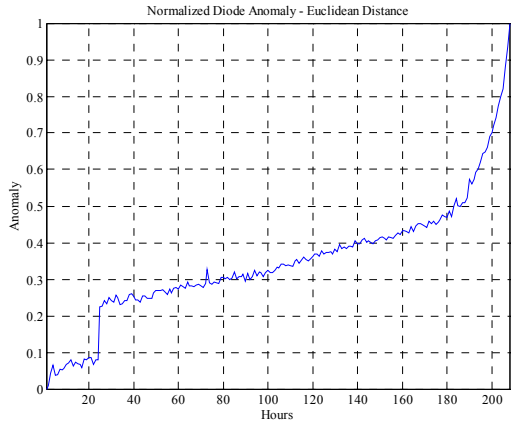

Figure 6: Anomaly Measure Generated from Diode Data – Euclidean Distance Metric – Test 1

In Figure 6, the jump in anomaly at 24 hours was a result from the end of the burn in period leading into the start of the accelerated testing. In general, the anomaly increases steadily until approximately 180 hours into the test where the degradation accelerates rapidly. The last data point was taken just over 200 hours when the converter failed.

The following figure combines the SD anomaly of Figure 6 with those obtained from an efficiency calculation and from the output voltage form factor.

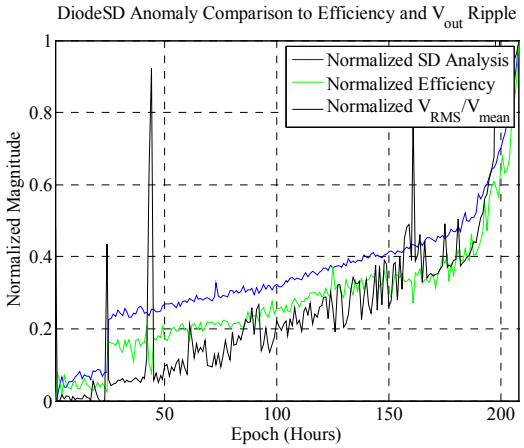

Figure 7: Comparison of Symbolic Dynamics Anomaly, Estimate Converter Efficiency, and Form Factor

As seen in Figure 7, the three measures compare well with one another. All three measures show some effect from the break in period into the accelerated testing. In this example, it is clear that Symbolic Dynamics reproduces the results of the other metrics with minimal effort. Additionally, the SD generated anomaly has less noise as compared to the other two measures over the complete test period. Forward thinking, this result should be positive for use in a prognostics sense with these converters

4.2 Second Converter Test

The testing was repeated with a second converter to reproduce the results seen above. The converter was again tested with a 24 hour burn in period and then left to be operated at 85°C until failure.

This test also resulted in failed input capacitors; however, the complete test lasted approximately 1,800 hours. Symbolic dynamics was again implemented on the diode data and the results are shown in Figure 8.

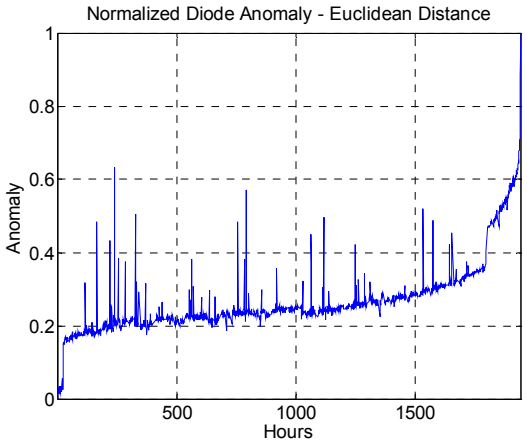

Figure 8: Anomaly Measure Generated from Diode Data – Euclidean Distance Metric – Test 2

In Figure 8, the test lasted significantly longer than the previous test. However, the results are very similar with the anomaly trend increasing rapidly toward failure. The jump in anomaly in the beginning is due to the break in interval while the jump towards the end (around 1,700 hours) was due to a change in the test parameters. At that point, the temperature of the test was increased from 85°C to 95°C in order to further accelerate the testing.

Again, we aim to compare our results to metrics more commonly used to diagnose the health of an electronic system. Using the same data, the efficiency and form factor metrics were calculated and the results are shown in Figure 9.

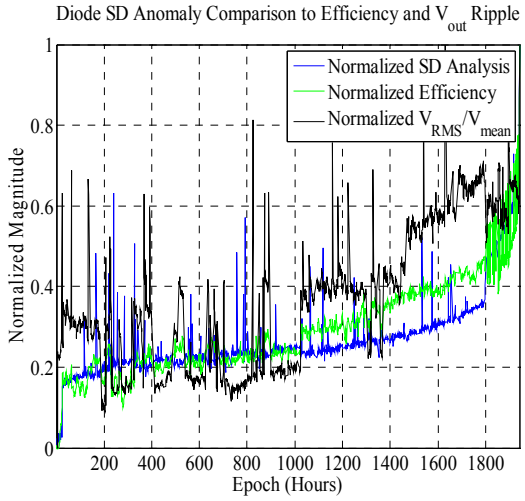

Figure 9: Comparison of Symbolic Dynamics Anomaly, Estimate Converter Efficiency, and Form Factor

As is observable, each of the measures are susceptible to the jump in operating temperature both from the break in period and from the increase in test temperature near the end of the test.

As compared to the results from the first test, the form factor metric does not produce as clear a trend as compared to the SD or the efficiency result. It would be difficult to determine current state of health from this trend.

Efficiency is a consistent metric between the two tests and is relatively easy to calculate. However, it does require one to record the input and output characteristics of the converter during operation whereas the SD methodology only requires the monitoring of one channel. The SD metric in both cases also produces a consistent degradation metric that could be used for diagnostics.

5. CONCLUSION

This paper proposes a data derived approach to monitoring dc-dc converters for degradation during operation. The methodology is based on Symbolic Dynamics that converts the captured time series data into a symbolic series that is analyzed statistically. The statistical results are then used to generate an anomaly based on the current operating conditions of the converter as compared to a known baseline.

The algorithm was tested on data recorded from two dc-dc forward converter tests. The aim was to capture degradation trends from the converters by monitoring the input voltage, switch current, MOSFET drain to source voltage, the output freewheel diode voltage, and the output voltage. It was determined that the diode voltage was the most sensitive to the internal degradation of the converter.

The generated anomaly from the SD algorithm was compared to the overall efficiency of the converter as well as the form factor of the output voltage. The form factor metric aims to capture the change in the output voltage ripple related to degradation of the output electrolytic capacitor.

The results show a consistent trend generated from both the SD anomaly and the efficiency of the converter. The form factor was inconsistent in generating trends between the two tests.

Future work will focus on effects to the algorithm from loading changes as well as further investigation into the effects of the different parameters in the Symbolic Dynamics algorithm. It was also determined that temperature deviations affect the data derived method which requires further investigation. Investigation of using the generated trends for prognostication will also be researched. The trends produced from testing currently have generated trends that we believe are applicable for life prediction.

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