Turn-off Time as a Precursor for Gate Bipolar Transistor Latch-up Faults in Electric Motor Drives

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ABSTRACT

In this paper, effects preceding a latch-up fault in insulated gate bipolar transistors (IGBTs) are studied as they manifest within an electric motor drive system. Primary failure modes associated with IGBT latch-up faults are reviewed. Precursors to latch-up, primarily an increase in turn-off time and junction temperature, are examined for the IGBT. In addition, the relationship between junction temperature and turn-off time is explained by examining the semiconductor properties of an IGBT. To evaluate the effects preceding latch-up, seeded fault testing is conducted using aged transistors induced with a fault located in the die-attach solder layer. Since junction temperature cannot be directly measured, the transistor turn-off time is used as a measured system parameter to correlate between healthy and fault conditions. The experimental results provide statistically significant evidence (within 99% confidence) that an IGBT latch-up event, caused by elevated junction temperatures, can be detected by monitoring the transistor turn-off time in-situ.

1. INTRODUCTION

In recent years, significant efforts have been put into developing fault-tolerant motor drive systems. Standard architectures follow two main principles, fault detection and fault compensation through active reconfiguration. In the first fault-tolerant motor drive reported by Janhs, the fault-tolerance was introduced by using multiple independent phase-drive units to feed a five phase machine (Janhs, 1980). A rule-based expert system based on the operator's response has been proposed by Debebe et al. for determining the fault devices in PWM-VSI drives (Debebe, Rajagopalan, & Sankaran, 1991). Other use of knowledge based systems for fault detection in motor drives has been presented in (Peuget, Courtine, & Rognon, 1998; Mendes & Marques, 1999). Inverter reconfiguration achieved by isolating and disconnecting the faulty switching component has been proposed in (Fu & Lipo, 1993; Bolognani, Zordan, & Zigliotto, 2000).

In all of these studies, reconfiguration is considered only after a hard fault has occurred, such as an open circuit or short circuit condition (Kastha & Bose, 1994). There is a lack of integrating detection, identification, isolation and fault reconfiguration into the design of the fault-tolerant motor drive system (Araujo Ribeiro, Jacobina, Silva, & Lima, 2004). Part of this is due to an absence of early indicators available during the design phase. If a fault mode can be predicted, or at a minimum anticipated, before it manifests into a hard fault (i.e. open / short circuit), then system reconfiguration can be achieved during normal operation. Reconfiguration under such conditions allow for safer mode transitioning.

The remainder of this paper is organized as follows. Section 2 investigates the device structure of IGBT devices and their associated failure mechanisms leading to the dominant mode of failure, latch-up. Section 3 presents an aging procedure used to generate and evaluate damaged IGBT devices corresponding to the latch-up fault mode. Section 4 describes a seeded fault experiment used to evaluate the effects of degraded IGBTs in a three-phase power inverter. Section 5 analyzes the data collected from the seeded fault experiment conducted on a three-phase power inverter using healthy and faulty transistors. Finally, Section 6 discusses the findings of this study and future work.

2. IGBT FAILURE ANALYSIS

The importance of IGBT module reliability has significantly increased due to the widespread use of these devices with a growing number of target applications, which includes power conversion and motor drives. IGBT modules are key components for current switching and, in particular, they can be used to control AC motors from DC supplies for urban and high-speed traction applications (Shammas, Rodriguez, Plumpton, & Newcombe, 2002). Large IGBT modules have very high current handling and blocking voltage capabilities in the order of hundreds of amperes and thousands of volts, respectively. In a typical IGBT-based motor drive, 4% of the controlled power is dissipated as heat within the de-

vice (He, Morris, Shaw, Mather, & 297., 1998). Thus thermal and thermal–mechanical management is critical for power electronics modules. The failure mechanisms that limit the number of power cycles are caused by the coefficient of thermal expansion (CTE) mismatch between the materials used in the IGBT modules (Ye, Lin, & Basaran, 2002).

2.1 Device Structure

An IGBT module is a four-layer structure, shown in Figure 1 (a). The common symbol used to represent an IGBT is illustrated in Figure 1 (b). The structure is similar to a metal-oxide semiconductor field effect transistor (MOSFET) except a heavily doped p-type layer is added. A pnp-type bipolar junction transistor (BJT) is formed with its emitter at the substrate and its collector, the p-type body region, connected to the top-layer metal. A parasitic npn-type BJT is also formed with its collector in the n-type epitaxial (epi) region and its emitter terminated at the top-layer metal (Russel, Goodman, Goodman, & Neilson, 1983). An equivalent circuit for the IGBT is also provided in Figure 1 (c). The combination of the two transistors produces a structure similar to that of a thyristor ("IGBT Characteristics", n.d.; Lidow & Herman, 1981).

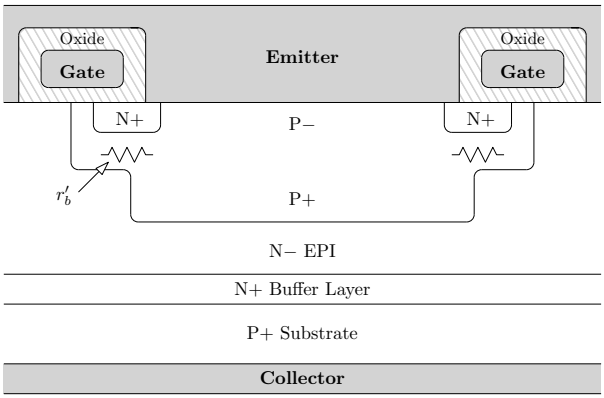
During normal IGBT operation, when a positive potential is applied across the gate-emitter and collector-emitter terminals, represented as V_{ge} and V_{ce} in Figure 1 (c), the MOSFET biases the BJTs to allow current to flow from the collector-to-emitter, denoted as I_c. However, when the IGBT is turned off abruptly by setting $V_{ge} = 0$, the turn-off current, $I_{c(\text{off})}$, decays slowly with a long tail. This is because excess holes in the epi-layer can only be removed by recombination (Huang, Gong, & Chen, 2002). Although the IGBT is superior to traditional power devices, the latch-up phenomenon arises which may occur due to the inherent thyristor structure (Huang et al., 2002).

2.2 Latching Failure Mode

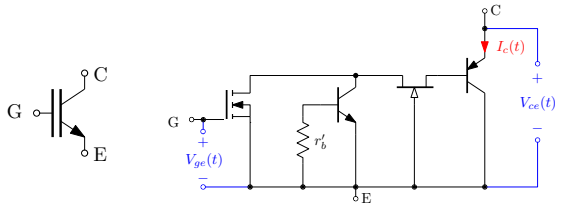
As described earlier, the four-layer structure of the IGBT resembles that of a thyristor. The thyristor is prevented from operating by limiting the gain of the two transistors and reducing the value of the parasitic resistance, r'_b. Under fault conditions, excess current can flow through r'_b as the MOSFET channel is reduced when attempting to turn-off the IGBT. This excess current can cause a voltage across r'_b that drives part of the IGBT structure into a latch condition (Chokhawala, Catt, & Kiraly, 1995). The collector current at which latch-up occurs is called the latching current. The magnitude of the collector current required to induce latch-up reduces with increasing device temperature. Hence, the susceptibility to latch-up is greater at higher device temperatures (Aoki, 1993). Once a latch-up event occurs, control of the IGBT from the gate is not possible.

2.3 Failure Modes

Mechanical construction of a semiconductor device determines its inherent reliability, not the electrical specification of the silicon, provided it is not operated outside its design limits. The mechanical construction includes the die, its mounting to the lead frame or module base, the connections from the die electrode pads to the



(a) IGBT cross section



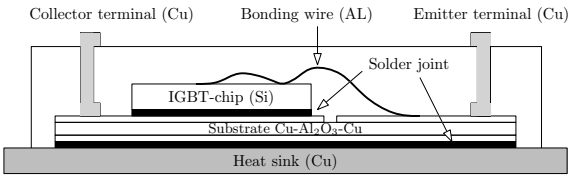
(b) IGBT symbol (c) Equivalent circuit.

Figure 1: Overview of an IGBT illustrating its (a) silicon cross section, (b) symbol and (c) equivalent circuit.

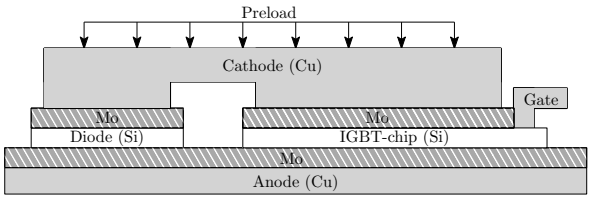
output leads or terminals and any molding compounds or infill materials used to protect the silicon from environmental contamination (*Industrial Level Qualification Requirements for Discrete Product*, 2010). During temperature cycling, the various mechanical parts making up the device expand and contract at different rates. Although every effort is used to select materials having closely matched CTEs, small differences are inevitable. Repeated temperature cycling eventually causes a device to fail through mechanical fatigue. The failure modes of IGBT modules are dependent on the mounting technology used. Common IGBT failure modes frequently reported in the literature are bond lifting (Malberti, Ciappa, & Cattomio, 1995; Sankaran, Chen, Avant, & Xu, 1997; Metrotra, He, Dadkhah, Rugg, & Shaw, 1999), and thermo-mechanical deterioration of the die attach layer (B. J. Baliga, 1996; Lambilly & Keser, 1993).

Wire Bond Lifting

For wire bonding IGBT modules, the emitter bonding wire lifting is reported as the leading failure mode (Ye et al., 2002). A cross section of a wire bonding package is shown in Figure 2 (a). Bonding wires are subjected to tensile stress due to the temperature excursions ΔT_j during power cycling (Somos, 1993). This is because the Al wire has a much larger CTE and expands during heating. Cova and Fantini cite degradation of the die attach layer as a driving factor for bond lifting (Cova & Fantini, 1998). Their conclusion is similar to that of Auerbach and Lenniger's (Auerback & Lenniger, 1997), that ΔT_j is the cause for damage of the soldering layers and bond wires and the power cycling lifetime is exponentially related to ΔT_j. According to Held et al., the number of



(a) Wire bonding IGBT module.



(b) Press-pack IGBT module.

Figure 2: Cross section of (a) wire bonding and (b) press-pack IGBT modules.

cycles to failure, N_f, of the wire bonds is a function of T_j and ΔT_j (Held, Jacob, Nicoletti, Scacco, & Poech, 1999),

$$N_f \propto (\Delta T_j)^{\alpha} \, e^{k_T / T_j}, \tag{1}$$

where α and k_T are real-valued constants.

Solder Die Detachment

For press-pack IGBT modules, degradation of the die attach solder layer is reported as the primary failure mode. The mechanical construction includes the silicon die, its mounting to the lead frame or module base, the connections from the die electrode pads to the output leads or terminals and any molding compounds or infill materials used to protect the silicon from environmental contamination (B. J. Baliga, 1996). The silicon die is soldered to the direct copper bonding (DCB) substrate, and the DCB is soldered to the copper heat sink, shown in Figure 2 (b). The substrate and heat sink have a much larger CTE than the silicon die. Cyclic temperature shifts during operation produce cyclic shear strains in the die bond due to the CTE mismatch between layers. This eventually produces cracking due to fatigue, which lower the critical capability of the bond to transfer heat generated in the die (Olson & Berg, 1979; Pecht, Dasgupta, Evans, & Evans, 1994). The loss of die bonds will increase the die temperature and effectively reduce the minimum latching current of the IGBT. Thus, the power transistor will eventually fail by catastrophic burn-out or secondary breakdown.

2.4 Aging Factors

It's accepted that real-life testing on IGBT devices shows their life expectancy to be related to T_j, ΔT_j and the case temperature T_c (Somos, 1993). Cova and Fantini advocate the use of power cycling as a stress test because the devices are operated in conditions similar to those encountered in the field (Cova & Fantini, 1998). Wu et al. recommend against power cycling citing its bias of a particular fault mode, bond wire detachment (Wu, Held, Jacob, Scacco, & Birolini, 1995). Instead Wu et al. prepared cross-sectional samples of several IGBT packages and applied thermal cycling stress. After aging, the samples were analyzed and shown to have developed voids and cracks in the solder layers. They conclude the damaged caused by thermal stress degrades the heat dissipation of the IGBT module. An alternative approach presented by Ginart et al. introduce a way to induce damage by applying power cycling until latch-up occurs (A. E. Ginart, Brown, Kalgren, & Roemer, 2009; A. Ginart, Brown, Kalgren, & Roemer, 2007). However, instead of continuing to induce short-circuit stress, the device is allowed to cool to room temperature before another latch-up event is induced. Under these stress conditions Ginart et al. were able to induce damage in the solder die layer in a shorter amount of time, as verified by Patil et al. (Patil, Celaya, Das, Goebel, & Pecht, 2009; Patil, Das, Goebel, & Pecht, 2008).

2.5 Aging Effects

Wire bond lifting and solder die detachment are a direct consequence of thermal degradation. Ginart et al. indicate the IGBT latching current reduces with the accumulation of thermal damage (A. Ginart, Roemer, Kalgren, & Goebel, 2008). They conclude this occurs as a result of an overall increase in T_j, which is consistent with (Ye et al., 2002). Its explained by Patil et al. that the overall increase in T_j is caused by increased thermal impedance as a result of the degraded die attach (Patil et al., 2009, 2008). Consequently, this change in temperature causes intrinsic device properties of the transistor to change. According to Hallen et al. , the thermal junction temperature is related to the lifetime of the minority carriers, τ_{HL}, injected into the N- region of the device during forward conduction (Hallen, Keskitalo, Masszi, & Nagl, 1996). The relationship between T_j and τ_{HL} is related by the following expression (Engström & Alm, 1978),

$$\tau_{\text{HL}} = \tau_0 \left(\frac{T_j}{300} \right)^{\kappa}, \tag{2}$$

where $\tau_0 > 0$ is the high-injection lifetime at $T_j = 300\,^{\circ}\text{K}$ and $\kappa > 0$. According to Baliga et al. , the increased minority carrier lifetime causes an increase in the transistor turn-off time, t_{off}, defined as (J. Baliga, 1985),

$$t_{\text{off}} = t_{90\%} - t_{10\%}, \tag{3}$$

where $t_{10\%}$ and $t_{90\%}$ correspond to the time when V_{ce} is 10% and 90% of its final value accordingly.

3. ACCELERATED AGING

3.1 Hardware Setup

During the aging process, the transistor's case temperature is controlled in a feedback loop to induce damage. This is achieved using a DAQ computer, current controller and an IGBT gate driver, shown in Figure 3. The DAQ computer regulates the junction temperature, T_j, of the IGBT by measuring temperature, and adjusting the applied collector current, I_c. The temperature is measured along the front and back surfaces of the semiconductor package, represented by $T_{c(\text{front})}$ and $T_{c(\text{back})}$, to estimate T_j using the thermal model provided by the manufacturer ("IRG4BC30KD datasheet", 2000). A current sensor is used as feedback for the current controller to regulate the PWM output to the gate driver. The gate

driver is used as a buffer between the IGBT and current controller. The aging process is accelerated by removing the heat sink from the transistor in order to elevate the junction temperature for lower set-point currents. During each test, the DAQ computer acquires measurements for $T_{c(\text{front})}$, $T_{c(\text{back})}$, V_{ge}, V_{ce}, I_c, and I_g.

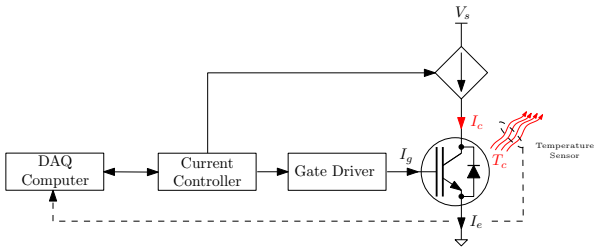


Figure 3: Block diagram of the accelerated aging platform.

3.2 Aging Procedure

The IGBT aging procedure consists of five stages: initialization, data acquisition and control, latch-up observation, latch-up recovery and repeat. An overview of the aging procedure is illustrated in Figure 4.

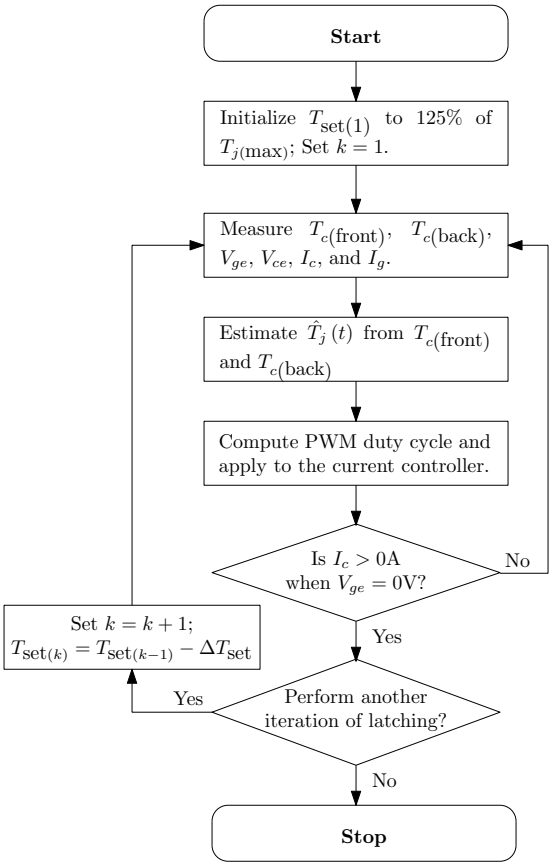


Figure 4: Flowchart of the accelerated aging procedure.

Initialization

The reference temperature is initially set at $T_{\text{set}(1)}$. In practice, $T_{\text{set}(1)}$ is established at 125% of the maximum operational junction temperature defined by the manufacturer.

Data Acquisition and Feedback Control

Measurements for $T_{c(\text{front})}$, $T_{c(\text{back})}$, V_{ge}, V_{ce}, I_c, and I_g are acquired using sensors connected to the DAQ computer. Estimates for $\hat{T}_j$ are computed from the measurements $T_{c(\text{front})}$ and $T_{c(\text{back})}$ using the thermal model provided by the manufacturer ("IRG4BC30KD datasheet", 2000). The set-point error $e(t) = T_{\text{set}(k)} - \hat{T}_j(t)$ is used in a proportional gain feedback control to arrive at a set-point to adjust the PWM applied to the IGBT. Measurements for V_{ge}, I_c, V_{ce} and I_g are acquired to detect a latch-up event.

latch-up Observation

When a latch-up condition occurs, the transistor is stuck in a permanent on-state. This is detected when $V_{ge} = 0$V and $I_c(t) > 0$A. During this event, the PWM signal applied to the transistor is disabled ($V_{ge} = 0$V). However, due to latching, the transistor cannot be successfully turned off and the temperature continues to rise.

latch-up Recovery

Manual interruption occurs to turn-off the collector current, I_c, to the transistor. During this phase the transistor is given sufficient time to cool allowing for a reduction in T_j.

Repeat

A decision is made to continue aging the transistor for another iteration of latching. If another latching event is desired, a new reference temperature is set for the k^{th} latching iteration where the change in reference temperature, ΔT_{set}, typically ranges from 10°C to 20°C.

3.3 Ringing Attenuation

The ringing feature, discussed in previous papers by Ginart et al. was used as a metric to verify permanent changes in the transistor after exposure to accelerated aging (A. E. Ginart et al., 2009; A. Ginart et al., 2007). Samples of previously aged components studied by Vital et al. indicated a correlation between damage of the solder-die attach layer and ringing attenuation (Patil et al., 2009, 2008).[1]

4. SEEDED FAULT TESTING

The seeded fault testing platform, designed as a small-scale electric power-drive system, was used to evaluate the performance of the power inverter when inserting faulty transistors.

[1]For additional information regarding the ringing attenuation metric and its correspondence to physical device damage, please refer to the papers by Ginart et al. and Patil et al. as cited in this section.

Table 1: Statistics of t_{off} for baseline and fault conditions. The mean and variance are provided for each data set along with the corresponding 90%, 95% and 99% confidence intervals.

Data set	Mean $[\mu s]$	Variance $[\mu s^2]$	CI (90%) $[\mu s]$	CI (95%) $[\mu s]$	CI (99%) $[\mu s]$
Baseline	0.1782	7.9210×10^{-5}	$(0.1635, 0.1929)$	$(0.1604, 0.1960)$	$(0.1552, 0.2012)$
Fault #1	0.2517	1.0816×10^{-4}	$(0.2345, 0.2689)$	$(0.2309, 0.2725)$	$(0.2249, 0.2785)$
Fault #2	0.2983	1.3689×10^{-4}	$(0.2790, 0.3176)$	$(0.2749, 0.3217)$	$(0.2681, 0.3285)$

4.1 Hardware Setup

A picture of the testing platform identifying the core components is provided in Figure 5. A laptop computer acquires test data from a data acquisition (DAQ) module and an oscilloscope using LabVIEW. The laptop computer also controls the digital motor controller and a programmable DC load using an RS232 interface. The digital motor controller interprets speed commands from the laptop computer and translates them into pulse-width modulation (PWM) signals. These PWM commands are sent to a three-phase power inverter connected to a 115VAC power source. The power-inverter modulates the PWM signals on the lines of a three-phase AC motor by using internal power transistors, more specifically IGBTs, to draw up to 6A of current at 115VAC. The shaft of the three-phase AC motor is mechanically coupled to a DC synchronous motor acting as a mechanical load. A load torque is applied by placing a programmable electric load on the output of the DC motor. Hall effect current sensors and voltage transducers are used to record current and voltage measured at the three-phase AC motor and DC motor.

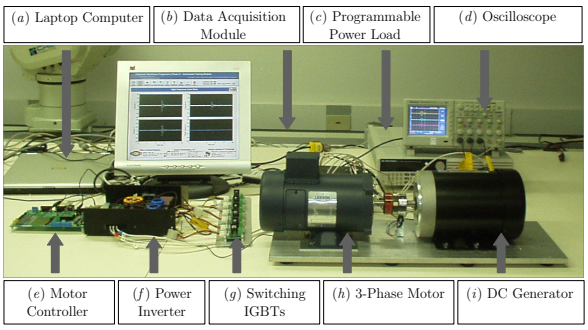


Figure 5: Photo of the experimental seeded fault test setup. The testing platform consists of: (a) laptop computer, (*b*) data acquisition module, (c) programmable power load, (d) oscilloscope, (e) motor controller, (f) power inverter, (g) switching IGBTs, (h) three-phase motor and (i) a DC generator.

4.2 Testing Procedure

Seeded fault testing was conducted by replacing selected components with degraded IGBTs in a power inverter. An electrical schematic of the power inverter connected to a three-phase induction machine is shown in Figure 6. The three-phase power inverter includes six IGBT components ($Q1$–$Q6$) used as switching transistors for DC-to-three-phase AC power conversion. In this setup, transistors $Q1$–$Q5$ are healthy (out of box) IGBT components and $Q6$ is replaced with either a healthy or faulty IGBT device.

Each test was conducted using the platform shown in Figure 5. During testing, the three-phase power inverter was operating within its normal operating conditions while driving a three-phase motor connected to a DC generator with an electric load. The experiment was conducted for a series of predefined static operating points by varying the speed of the motor and the load on the generator. The speed was evaluated at 800, 1000 and 1200RPM with a fixed motor current of $1\,\text{A} - \text{RMS}$. During this particular experiment the dead-time between each transistor switching cycle was increased from $2\,\mu s$ (the default) to $4\,\mu s$ to prevent potential switching failures from occurring. Measurements for the transistor turn-off time were acquired by measuring V_{ce} across transistor $Q6$ using a Tektronix TBS2024 oscilloscope. The measurement was synchronized on the negative edge of the control signal driving the gate of transistor $Q6$. The turn-off time was computed from the acquired waveforms using (3).

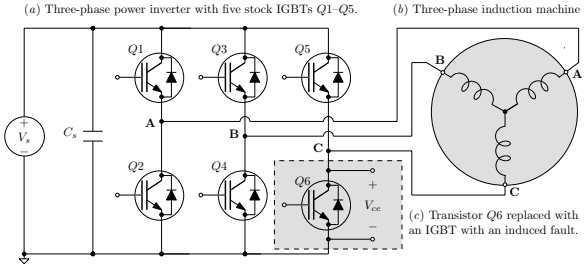


Figure 6: Electrical schematic of the seeded fault testing platform. Shown is the (a) three-phase power inverter wired to a (b) three-phase induction machine where (c) transistor $Q6$ is replaced with either a healthy or faulty transistor.

5. EXPERIMENTAL RESULTS

A set of eight transistors was evaluated during seeded fault testing. Of the eight transistors, two transistors were aged by following the procedure in Section 3. The remaining six transistors were in a presumably healthy or (out-of-box) condition. After aging two of the eight transistors, the fault status of each transistor was evaluated using the ringing attenuation metric discussed in Section 3.3. Samples H01–H06 correspond to healthy transistors while Fault #1 and Fault #2 correspond to faulty transistors accordingly. The ringing response for eight distinct transistors is shown in Figure 7. The plot labeled 'Healthy (baseline)' was generated from the mean value of six healthy transistors. The remaining two plots labeled 'Fault #1' and 'Fault #2' were acquired from two distinct IGBTs after undergoing accelerated aging. The ringing attenuation metric confirmed the six transistors

presumed to be new showed no indication of damage, whereas the two aged transistors produced indications of a fault in the die-attach layer.

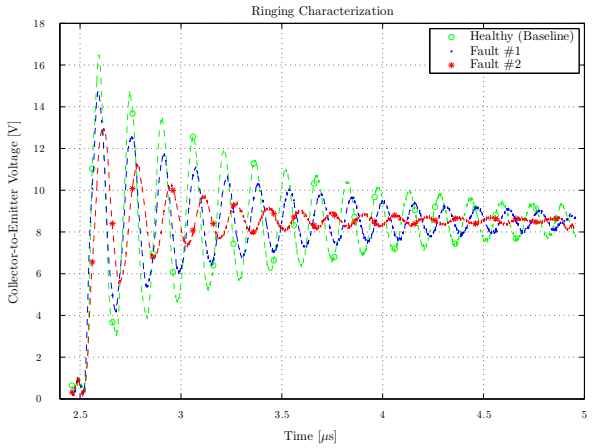


Figure 7: Time-series plots comparing V_{ce} measured for six healthy transistors (baseline) and after accelerated aging of two faulty IGBTs.

After fault verification, each transistor was subjected to seeded fault testing as described by the testing procedure in Section 4.2. According to the data, there is no statistical significance between the turn-off times of different healthy transistors. Therefore, this was used as baseline data to compare healthy and faulty transistors. The computed baseline values for t_{off} followed a normal distribution as illustrated in Figure 8, with a mean of $0.1782\,\mu$s and standard deviation $0.0089\,\mu$s. In addition, the computed t_{off} values for the faulty transistors also followed a normal distribution. The mean, variance and confidence intervals of t_{off} are presented in Table 1 for each data-set. According to the data, it can be shown with 99% confidence that t_{off} is greater for the faulty transistors under the same operating conditions.

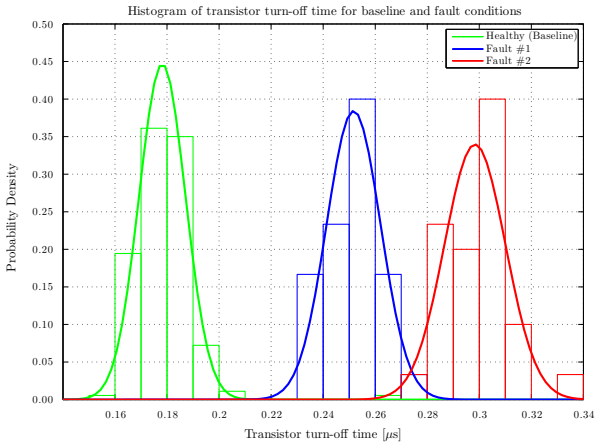


Figure 8: Histogram of t_{off} for six healthy transistors (baseline) and two faulty transistors.

6. CONCLUSION

This paper studied the effects preceding a latch-up fault in IGBTs for an electric motor drive system. Precursors to the primary failure mode, latch-up, were identified and modeled for the IGBT. Experimental seeded fault testing demonstrated the ability to distinguish between aged and healthy transistors using on-line measurements of transistor turn-off time during switching cycles. Statistical results were provided to verify these claims. Future work includes the development of an integrated diagnostic circuit module to monitor the turn-off time of each individual transistor as early fault indicator for latch-up.

ACKNOWLEDGMENT

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NOMENCLATURE

I_c	IGBT collector current	A
I_e	IGBT emitter current	A
I_g	IGBT gate current	A
I_m	Motor current	A
N_f	Cycles-to-failure	–
T_c	Case temperature	°K
T_j	Junction temperature	°K
V_{ce}	IGBT collector-to-emitter voltage	V
V_{ge}	IGBT gate-to-emitter voltage	V
V_s	DC bus voltage	V
k_T	Thermal model constant	°K
r'_b	Parasitic resistance	Ω
t	Time	s
t_{off}	IGBT off-time	s
α	Thermal cycling parameter	–
κ	Thermal modeling parameter	–
τ_{HL}	High-level injection lifetime	s
τ_0	High-level injection lifetime at $T_j = 300\,°\text{K}$	s

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