A Fault-Tolerant DC-DC Converter with Zero Interruption Time Using Capacitor Health Prognosis

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ABSTRACT

A high-end critical electronic system is expected to have hundreds of electronic subsystems which rely on the Power Management Unit (PMU) to be energized. Having an efficient PMU is crucial and it requires reliable and well-structured voltage buck converters to translate the supplied voltage levels. The buck converters employed in PMU are expected to be fault tolerant and supply uninterrupted power while serving critical subsystems. Active redundant parallel buck converters employed in PMU to achieve fault tolerance increases overhead in terms of area, cost and power dissipation. In this paper, a DC-DC converter is designed for the PMU by combining two legs of buck converters with an effective output of 3.3 V. A simple yet effective technique is proposed to design a fault-tolerant buck DC-DC converter by bypassing a faulty converter leg. The proposed system utilizes an online signal processing-based method for prognostic fault detection. Ripple content in the voltage of the output Aluminum Electrolytic Capacitor (AEC) is monitored and used as a primary health indicator for the primary buck converter leg. Increase in the output ripple due to degradation is used for the prognosis of primary converter failure. The secondary buck converter leg is activated only upon the confirmed prognosis of a faulty primary converter leg to avoid false triggering. The timely prognosis of primary converter failure and activation of secondary converter facilitates uninterrupted power supply. An experimental setup is built and tested in the laboratory. Experimental results indicate a smooth transition from the primary converter leg to the secondary demonstrating an uninterrupted power supply along with the simplicity and effectiveness of the proposed solution.

1. INTRODUCTION

The digital revolution, enhanced connectivity and new technologies are fostering innovation, revolutionizing industries, improving efficiency and impacting several sectors of the economy. Technology is always improving, and critical applications, whose reliable functioning is essential to system operation, are becoming more and more integrated into our society. The critical applications market has seen a never-before demand for safe and robust systems in the modern period.

This reinforces the importance of prioritizing dependability, security, and stability to ensure that these critical systems continue to operate without interruption (Zhang, Zhang & Chen, 2019).

All these systems will demand different power supply ratings to function. The required power levels for each subsystem are provided by the Power Management Unit (PMU) which is attached to its main supply. Figure 1 depicts the block diagram of an electronic system focusing on PMU (Sharma & Tippeswamy,2019). The PMU must supply a specific uninterrupted voltage to subsystems so that each subsystem functions reliably. Thus, having fault-tolerant DC-DC converters is one of the primary requirements in critical systems. Due to this fact, this paper intends to discuss fault-tolerant DC-DC converters in buck configuration for critical applications. Power semiconductor switches and Aluminium Electrolytic Capacitors (AEC) are the two major components of buck converters (Yarmunja, Sharma, & Nandihalli, 2016). Regretfully, 21% and 30% of breakdown or malfunctioning of power electronic converters are recorded due to a fault in the semiconductor switch and AEC, respectively (Sharma & Tippeswamy,2022). These components in the power supply may fail due to over-current, over-voltage, temperature increase, short-circuit, track breaking, etc. Also, in some cases, the cause of failure is unknown (Yarmunja et al., 2016) So prognostically identifying the failure of power converters and providing fault-tolerant systems in critical applications is crucial.

A fault-tolerant DC-DC converter is defined to function reliably despite the occurrence of a fault (Sharma & Tippeswamy, 2021). Fault -tolerance in a DC-DC converter is achieved in several stages like fault detection, fault diagnosis, and feasible fault- tolerance implementation.

Fault detection and diagnosis give an effective indication of the fault and status of fault. Approaches used for fault detection and diagnosis are majorly classified as data-driven, model-based, and knowledge-based methods (Sharma & Tippeswamy, 2021). Data-driven methods are

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also termed as signal processing methods. In this, either the time domain or frequency domain signature of identified signal parameters like DC bus current or capacitor voltage are processed to diagnose the fault (Sharma & Tippeswamy, 2021; Geddam, & Elangovan, 2020; Bento, & Cardoso, 2018; Sharma & Tippeswamy,2019). In model based and knowledge-based techniques, the system behavior is modelled in prior and consistency between expected and measured values are analytically examined (Sharma & Tippeswamy, 2021).

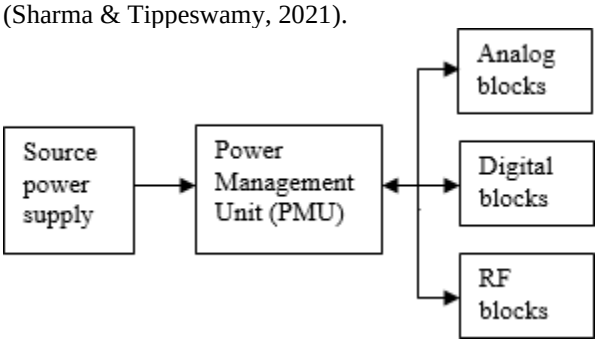


Figure 1. PMU powering sub circuits

The type of fault-tolerant strategy adopted is responsible for continuous power supply with admissible quality post fault detection. Fault-tolerant strategies are classified majorly as those which use additional hardware or those which are free of additional hardware (Sharma & Tippeswamy, 2021; Geddam, & Elangovan, 2020; Bento, & Cardoso, 2018). Strategies based on additional hardware use bypassing of a faulty module, inclusion of additional discrete components, or inclusion of redundant legs. Strategies without additional hardware utilize phase shift adjustment or bypassing of faulty modules (Sharma & Tippeswamy, 2021; Geddam, & Elangovan, 2020; Bento, & Cardoso, 2018). Hybrid methods of fault detection, diagnosis, and tolerance implementation are also demonstrated (Geddam & Elangovan, 2020). In this paper, a fault-tolerant buck converter for critical applications is proposed. Time domain signal processing is used for prognostic fault detection and diagnosis using additional discrete components. A hybrid fault tolerant strategy with the inclusion of redundant legs and discrete components is used to achieve fault – tolerance. The redundant leg is activated only upon the prognosis of primary converter leg failure.

The remainder of this paper is as follows. In section 2 a short survey of the available literature is carried out. Section 3 explains the methodology of the proposed solution. Section 4 validates the proposed solution with experimental results followed by a discussion. Finally, in Section 5, the overall work is concluded.

2. LITERATURE SURVEY

The primary solution to obtain a fault-tolerant power supply is by adding redundancy. The redundancy could be in terms of additional legs or additional components. An N+1 power converter is deployed in which N systems are required to run the system effectively (Zhang & Jiang, 2008; Nesgaard, & Andersen, 2004; Newark). Necessary and redundant systems are connected in parallel and diode ORing is used (Newark). In (Texas instruments) FET (Field Effect Transistor) ORing technique is proposed which reduces the voltage drop across the diode. Despite the additional benefits, when additional redundant systems are used parallelly, they increase the area, impose additional cost and dissipate more power. (Kumar & Rajpurohit, 2020) proposes a fault-tolerant boost converter by using two power semiconductor switches instead of one. In this, both switches share operating frequency equally and a control scheme is developed which adjusts the switching frequency to one switch if the fault is detected in the other. However, this solution leads to interruption in the output and works only for Boost converters. A simple fault clearance solution is proposed in (Rahimi, Jahan, Abdadifarad, Akbari, Ghavidel, Farhadi, Hossein, 2021). Here, with the help of one diode and fuses faulty switch is cleared, so that the redundant switch can take over. In this solution, the short circuit is cleared instantly with the help of a switch and the open circuit fault is eliminated using a diode and a fuse. The proposed solution is supported by simulation and experimental results only on a boost converter. In this case fault tolerance is implemented with static redundancy.

In many solutions key component failure leading to system failure is identified and signature of those components is studied. Parameters like inductor current, capacitor voltage, voltage between drain and source terminals of the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) switch, input current and output voltage ripple are analyzed and monitored for fault detection. (H. Givi, E. Farjah and T. Ghanbari, 2019) proposed and online fault detection method by monitoring voltage across the switch and capacitor ESR (Equivalent Series Resistance). The monitoring is achieved with the help of electrical and temperature sensors. References (Jagtap & More, 2020; Jagtap & More, 2020) deals with fault detection and tolerance by monitoring inductor current variation. An event counter is used to latch and activate the redundant switch. But this works only for open circuit faults during the ON state of the semiconductor switch. In (Dhananjaya, M, Padmanaban, Almakhles, & Potnuru, 2021), a fault-tolerant Dual Input Single Output (DISO) DC-DC converter is proposed. Inductor currents and input voltage are monitored to diagnose the fault. The proposed method demonstrates fault -tolerance towards power switch SC (Short Circuit) fault and input OC (Open Circuit) faults. Multiple redundant legs are employed and all legs are alternatively utilized under normal operation. Upon fault detection, healthy leg's duty cycles are reconfigured to continue the operation effectively. Here, multiple active redundant legs lead to power losses and system overheads.

In certain solutions to fault tolerant power supplies, bridge type or multi- level converters are used. Upon failure of one leg in the bridge or failure in one level, healthy parts are rearranged to continue operation. References (Costa, Buticchi, & Liserre, 2017; Costa, Buticchi, & Liserre, 2018) proposes a fault-tolerant strategy using a voltage doubler. In these, series resonant DC-DC converters are considered and upon one switch fault in the full bridge, the converter functions in the half-bridge mode. To compensate for the decreased voltage, a voltage doubler is used. Though this solution is simple it leads to efficiency compromises in constant uninterrupted output delivery.

Modern solutions using sensor components and solutions involving complex processors are also explored. (E. Jamshidpour, P. Poure, E. Gholipour and S. Saadate, 2015) proposed a fault tolerant scheme by monitoring inductor current and using FPGA (Field Programmable Gate Array) based fault detection. Here OC fault is cleared immediately using a redundant switch and SC fault is cleared by reconfiguration leading to interruption in the output ranging to maximum 500us. In (Xu & Chen, 2021) a new cost-effective fault-tolerant scheme without redundant switch is proposed for photovoltaic (PV) systems with Maximum Power Point Tracking (MPPT). In this Differential Power Processing (DPP) converter submodules coordinates are adjusted upon fault detection and boost converters PWM (Pulse Width Modulation) is controlled to have a fault-tolerant operation. This solution is complex and works only for OC faults. In reference (Soon, Lu, Peng, & Xiao, 2020) a new fault- tolerant scheme is proposed with an additional redundant switch. The fault is detected by measuring the voltage across the drain-source terminal (Vds) of the MOSFET switch. The reconfiguration of converter post fault is enabled using an affine-parametrization-based control design implemented on a microcontroller. The method proposed is evaluated using the Markov model and through experiments. The proposed solution involves 10ms of interruption in the output of buck converter. (Li, Pan, Su, & Zhao, 2019) proposed a model-based method to detect sensor faults in buck controllers. Here, fault detection and fault-tolerant control are based on an affine switched system. The residual signals are identified for buck converter using switched system modeling. Fault detection is achieved by comparing the residual signal with a predefined threshold. System reconfiguration is also modeled and demonstrated through simulations for open circuit faults, gain and noise variations. However, proposed solution is complex in modeling.

Fault tolerant systems without additional hardware is also explored in literatures. This type of solution is mainly applicable in systems involving multiple legs where the phase shift is adjusted to continue operation. In systems with master slave arrangements the roles of master-slaves are rearranged to continue operation.

Reference (Figueiredo, Monteiro, Afonso, Pinto, Salgado, Cardoso, Nogueira, Abreu, Afonso, 2021) conducted a survey in which parallel, hybrid, and cascade architectures of buck converters were designed for various input and output voltages, and their efficiencies for LiDAR (Light Detection and Ranging) applications of autonomous vehicles were compared. (Figueiredo, et al., 2021) utilized LM series buck converters from Texas Instruments in their design. (Figueiredo, et al., 2021) discussed a design with 15V input, 3.3V output, and 1A load current for which the converter efficiencies were recorded at 92%,97%, and 91% for parallel, hybrid, and cascade architectures respectively.

3. METHODOLOGY

3.1 Capacitor Health Prognosis in Buck Converter

A DC-DC power converter in buck topology majorly has an inductor, a capacitor, a free-wheeling diode, and a semiconductor switch. Based on the control of the duty cycle of the semiconductor switch, the output voltage is defined. Standard semiconductor ICs (Integrated Circuits) are available to design buck converters. The components in the buck converter get degraded upon aging, leading to non-favorable operation. According to the literature, about 30% of power converter failures are due to AEC failures. From literature, capacitors are considered degraded when their capacitance reduces by 20% or ESR increases to 2.8 times the initial value (Kulkarni, Biswas, Koutsoukos, Celaya, & Goebel, 2010). (Sharma & Tippeswamy,2022) described, when an AEC degrades, the ac ripple content in its constant DC output increases. Here, a theoretical study of variation in the output ripple is performed by considering Arrhenius equation for variation of ESR with degradation as given by Eq. (1).

$$\frac{1}{ESR(t)} = \left(\frac{1}{ESR(0)}\right)\left\{1 - k * t * exp\left(\frac{-E}{(T+273)}\right)\right\} \quad (1)$$

where ESR(t) is the ESR value at time 't', T is the temperature in degrees Celsius at which the capacitor functions, t is the period of operation, ESR (0) is the initial ESR value at t = 0, k is the constant that depends on the design and construction of the capacitor, and E equals 4700.

An external capacitor is used in the design of a voltage regulator. The ESR of the capacitor is modified to emulate the degradation of the capacitor using Eq. (1). Degradation study is performed by measuring the variation of AC ripple in a steady DC output voltage. A reference generator is designed to set a threshold value of the output voltage ripple equivalent to 2.8 times the rise in ESR value at which the capacitor is considered degraded.

3.2 Fault Tolerant Buck Converter Design Using Capacitor Health Prognosis

In the proposed online fault tolerance method, two buck converters are used with the diode OR ing technique

(Newark). Figure 2 depicts the block diagram of the proposed method. The first buck converter i.e, primary

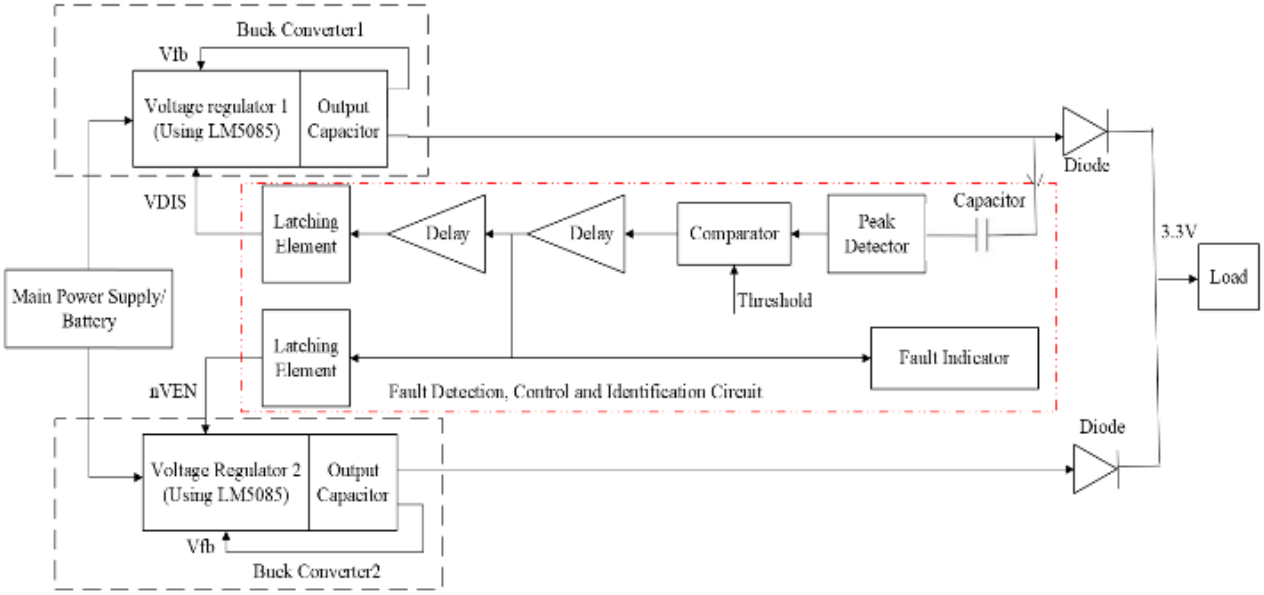


Figure 2. Block diagram of proposed solution.

regulator, is initially ON and gives a 3.3V constant DC output voltage. The AC ripple across the output capacitor is continuously monitored. The peak voltage of the AC ripple is extracted using a peak detector. The ripple peak extracted is compared with a predefined threshold (Sharma, & Tippeswamy, 2022) for prognostic identification of Buck Converter1 failure. When the AC ripple increases and reaches the threshold, the comparator switches the output. The comparator output is delayed using an RC (Resistor- Capacitor) network to avoid false triggering. The gradual increase in the voltage across RC network confirms the increased ripple. After the prognosis of Buck Converter1 failure, turn-ON of Buck Converter2 and turn-OFF of Buck Converter1 is initiated. Turn-ON signal is latched to Buck Converter2 and turn-OFF signal is latched to Buck Converter1 respectively.

An additional delay is introduced to the turn-OFF signal before latching to Buck Converter1 which assures turn-ON of Buck Converter2 first and turn-OFF Buck Converter1 later. This aids in providing an uninterrupted power supply

to the load without keeping the redundant buck converter always active. By activating the redundant buck converter only on a need basis, the overall power dissipation is reduced. When static power dissipation reduces, the degradation of other elements in the system is unaffected. This also increases the lifetime of the system and increases the reliability of PMU in an electronic system. A fault indication signal is provided for servicing purposes. Each block's basic functionality is described in the following section.

Buck Converter1 is considered as the primary regulator and Buck Converter2 is considered to be a redundant regulator. Here, each regulator is given the feedback voltage 'Vfb'. Feedback 'Vfb', adjusts the duty cycle of the semiconductor switch to maintain the specific output voltage. 'Vfb' is extracted from the respective converter's output. A peak detector is designed using operational amplifier which extracts the peak value of the ripple in the DC output. An operational amplifier based peak detector is used which continuously generates the ripple peak. The extracted ripple peak is an analog signal. This peak ripple value is compared against the predefined threshold. A threshold is set to a voltage that is equivalent to expected rise in the ripple when capacitor ESR increases to 2.8 times original value. If the ripple peak exceeds the threshold, the comparator switches the output. RC circuit-based delaying elements are designed. A latching circuit is designed using transistors to latch the enable signal (nVEN) to Buck Converter2. This latch maintains the enable signal even after Buck Converter1 turns off and peak ripple output reduces. A fault indicator is given which grants real-time fault indication. Turn-OFF of Buck Converter1 is delayed slightly using an RC network so that, Buck Converter2 turns on before turning off of Buck Converter1. A transistor-based latching circuit is used to latch the disable signal (VDIS) to Buck Converter1. The fault indicator signal and VDIS signal are independent of each other. The fault indication is done in real time as the fault is prognostically identified. However, VDIS signal has an additional predefined delay to assure turn- ON of Buck Converter2 prior to turn- OFF of Buck Converter1. Figure 3 depicts the flow chart of implementation of proposed fault tolerance method.

The proposed system monitors the increase in the capacitor output ripple due to capacitor degradation while

the system is functioning. Since, it is a prognosis method it can detect both OC and SC faults if the fault is due to capacitor aging.

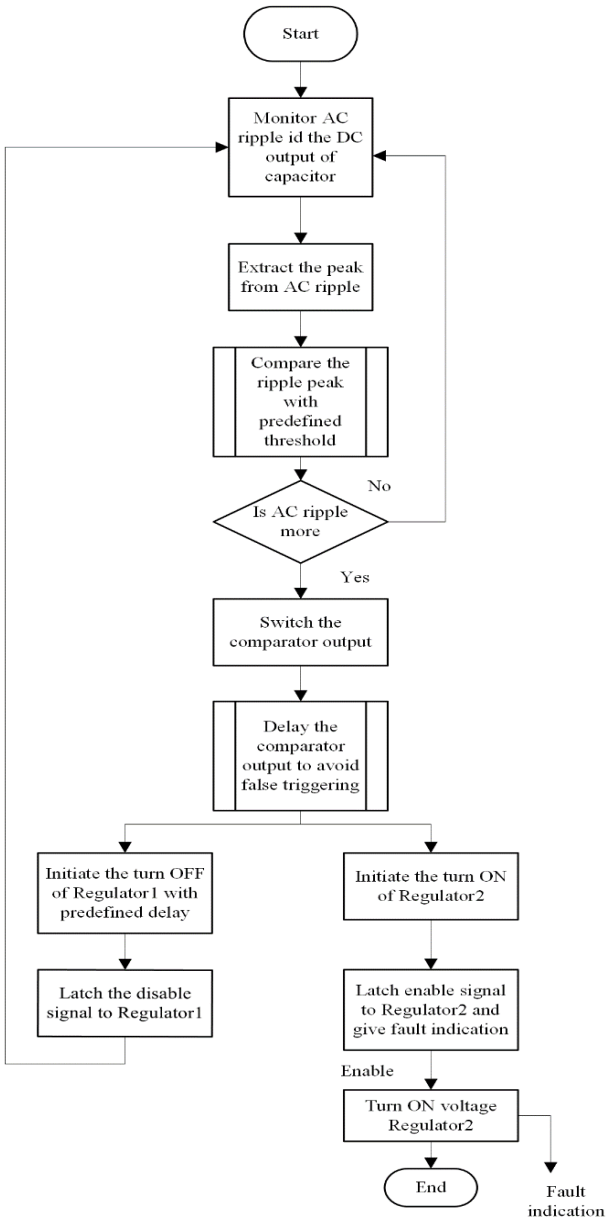


Figure 3. Signal flow chart of proposed methodology. Here, the threshold is defined with respect to 2.8 times increase of the ESR value from initial value.

3.3 Simulation and Experimental Tests

TINA by Texas Instruments is used to design and simulate the proposed solution. Table 1 a) depicts the major specifications assumed for the design of the proposed fault-tolerant buck converter. Table 1 b) lists the major components used in the design and experimental setup of the proposed system.

Parameter	Description	Value
Vcc	Input Voltage	12±3 V
Vout	Output Voltage	3.3V
Iout	Output Current	1A
Fs	Switching Frequency	500kHz

Table 1 a) Specifications of the proposed system

Component	Description
LM5085	Buck Switching Controller IC
CSD4502Q3A	Power MOSFET
B530C	Diode
L1, L2	4.3uH Inductor
C1, C2	33uF Output AEC
RL	3.3Ω Load Resistor
LST67K-J1L2-1-Z	LED Indicating Degradation
BC847 * 2N2605 ** TLV9062 ***	NPN Transistors*, PNP Transistors**, Op-amp***-Used in Fault Detection, Control and Indication Circuit.

Table 1 b) Components used in the proposed system.

The design makes use of a 33uF, 250mΩ (ESR) AEC by Nichicon Corporation as the external capacitor, Cout. In simulation, the ripple in the constant output of the capacitor is recorded for initial conditions. The capacitor ESR is then updated with the help of Eq. (1) to emulate degradation and varied ripple in the output is measured. The process is repeated until the ESR reaches 2.8 times the initial value of the capacitor. Considering a buffer value, threshold for degradation of the capacitor is fixed at 2.7 times increase of the ESR from its original value.

Figure 4 exhibits the prototype of the proposed fault tolerant buck converter solution. Figure 4 depicts various sub modules of the proposed system. Figure 5 displays the experimental setup used to validate the solution proposed. Here, a DC power supply is used to input 12 Volts of DC into the circuit. A digital oscilloscope is used to capture the signals. An external resistor is appended to increase the ESR of the AEC.

In experimental design, a 33uF, 250mΩ (ESR) AEC by Nichicon Corporation as the external capacitor, Cout. A relay component is used to increase the ESR thereby emulating the degradation of the capacitor. Here, maximum switching frequency of the regulator assumed in the design is 500kHz. So, 2us is minimum period. To provide a reasonable delay so that false triggering is avoided, a delay of 3.3ms is considered.

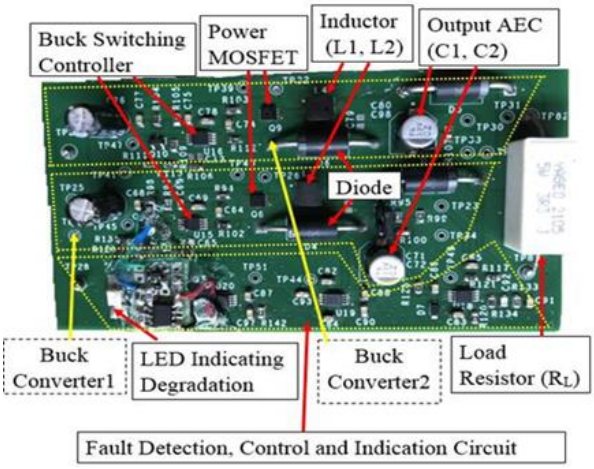


Figure 4. Prototype of proposed solution

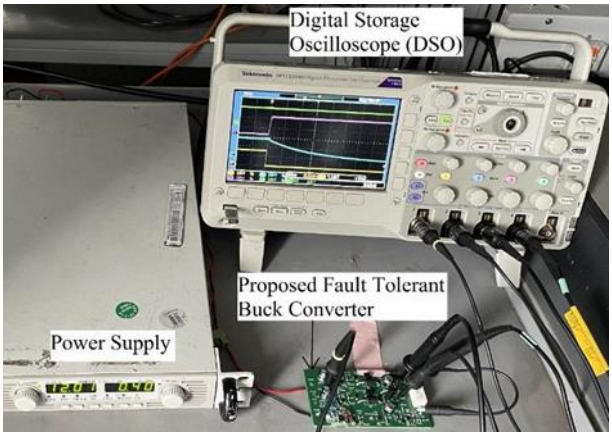


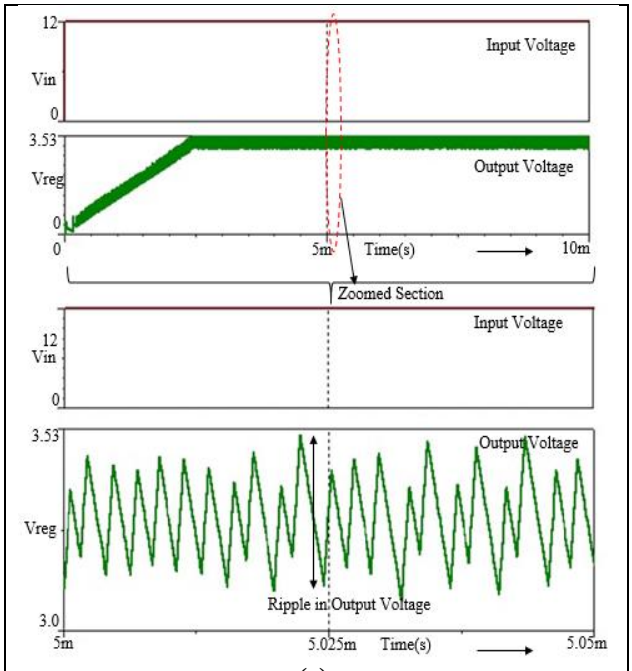
Figure 5. Experimental set-up of proposed system

4. RESULTS AND DISCUSSION

The performance of the proposed fault tolerance scheme when the system performs in steady state, while transitioning to degraded state and when recovers from faulty conditions is evaluated using simulations and through experimental evaluations. As capacitor degrades the effective capacitance decreases and ESR increases. The degradation of capacitor is directly related to aging of the capacitor. Thus here, degradation is measured with time. Table 2 lists the variation of ESR, effective capacitance and output ripple with time. For increase in the ESR due to degradation, the increase in the ripple is plotted in Figure 6. The voltage ripple observed for initial condition of AEC was about 0.33V. From Figure 6 it can be observed that, as capacitor degrades, the magnitude of the output ripple increases whereas the frequency of the ripple is not affected. From Figure 6 (b) it can be observed that the ripple increased to 0.89V when the ESR increases to 2.8 times the initial value. Figure 6 (c) depicts the variation of output ripple with degradation. A threshold equivalent to 2.7 times increase in the ESR is considered which is indicated in Figure 6 (c).

Time (Hours)	ESR(t) Ω	Ceff(with time) uF	Voutripple (V)
0	2.50E-01	3.30E-05	0.33
1000	2.62E-01	3.27E-05	0.35
2000	2.75E-01	3.23E-05	0.36
3000	2.89E-01	3.20E-05	0.36
4000	3.05E-01	3.17E-05	0.37
5000	3.22E-01	3.14E-05	0.39
6000	3.42E-01	3.10E-05	0.45
7000	3.64E-01	3.07E-05	0.45
8000	3.90E-01	3.04E-05	0.46
9000	4.19E-01	3.00E-05	0.47
10000	4.53E-01	2.97E-05	0.52
11000	4.94E-01	2.94E-05	0.54
12000	5.42E-01	2.90E-05	0.6
13000	6.00E-01	2.87E-05	0.65
14000	6.72E-01	2.84E-05	0.72
15000	7.65E-01	2.81E-05	0.86
16000	8.86E-01	2.77E-05	0.89

Table 2. Output Ripple Variation with Aging of Simulated AEC



(a)

Figure 6 a) Simulation results. Voltage ripple at the output when the capacitor is in initial conditions.

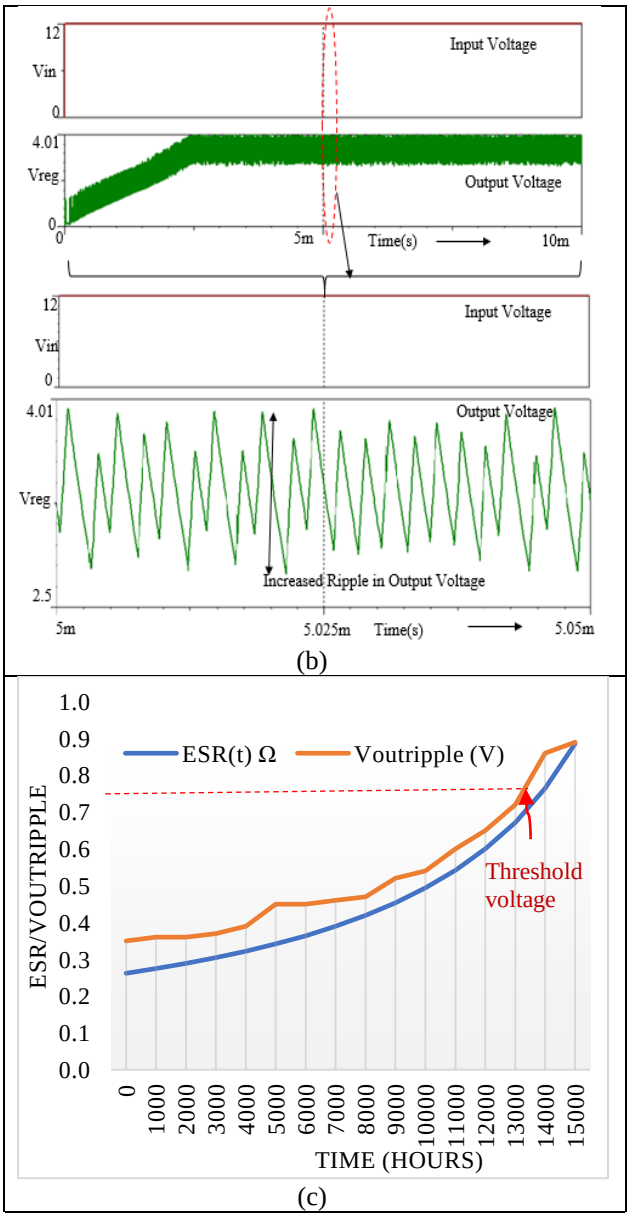


Figure 6. Simulation results. (b) Voltage ripple at the output when the capacitor ESR is increased to 2.8 times the initial value. (c) Variation of ripple at the output capacitor with degradation.

Figure 7 depicts the simulation results of proposed fault tolerance solution. The transient section is zoomed in and presented for better understanding. Here, there is no interruption time observed when the system switches from Buck Converter1 to Buck Converter2. We can observe in Figure 7 as the ripple in Buck Converter1 output increases due to degradation, enable signal nVEN to Buck Converter2 is activated first and with predefined delay disable signal VDIS to Buck Converter2 gets activated. The signal Vfault that indicates the fault in Buck Converter1 gets activated. From the simulation, it is observed that, when Buck Converter2 turns ON, switching MOSFET of Buck Converter2 adjusts its turn ON periods to attain the required output voltage gradually. The output voltage ripple reduces to normal after the turn-ON of Buck Converter2.

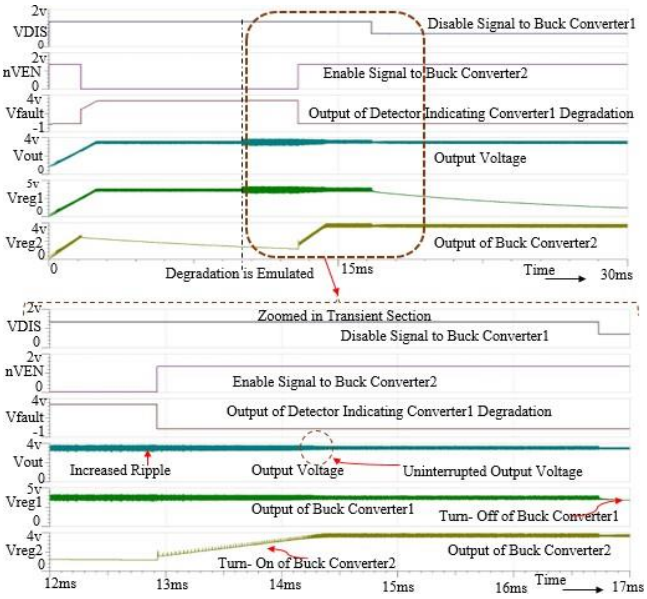


Figure 7. Simulation result of the proposed method. Here, Vreg1 and Vreg2 are the output voltages from Buck Converter1 and Buck Converter2 respectively. Vfault is the fault indicating signal. nVEN and VDIS are enable signal given to Buck Converter2 and disable signal given to Buck Converter1 respectively

Figure 8 depicts the experimental observations of proposed system for different probable conditions. Figure 8 a) displays output when the system turns ON and is functioning without any degradation. We can see from Figure 8 a) that upon turning ON, both Buck Converter1 and Buck Converter2 turn ON. After initialization Buck Converter2 turns OFF and Buck Converter1 continues to perform steadily and gives constant output voltage. Figure 8 b) displays the experimental result of the proposed system when a fault occurs during steady state operating conditions. The figure also displays the zoomed version of the output depicting the transition from Buck Converter1 to Buck Converter2. From the output waveform, we can observe the increase in AC ripple in the 3.3V DC output as the capacitor ESR is increased. This increased ripple is monitored and as it increases beyond the defined threshold, we can observe a shift in the output signal of Buck Converter2. Figure 8 b) also depicts the signal indicating the degradation of Buck Converter1 and gradual turn OFF of Buck Converter1. Here, initially, the system is tested for original capacitor parameters. Later, the capacitor ESR is updated by increasing the ESR emulating the degradation. Then the output changed as expected to the degraded version and fault detection and fault-

tolerance by activating Buck Converter2 is achieved. From Figure 8 b), we can observe that there is no interruption while switching from Buck Converter1 to Buck Converter2. Figure 8 c) displays output waveforms during the initial startup when Buck Converter1 is already degraded or faulty. In Figure 8 c) we can observe that upon turn-ON both Buck Converter1 and Buck Converter2 are activated. However, as Buck Converter2 begins to turn OFF the output ripple is monitored and immediately Buck Converter2 turns ON and Buck Converter1 turns OFF. We also observe that there is no interruption in the output voltage in any discussed conditions.

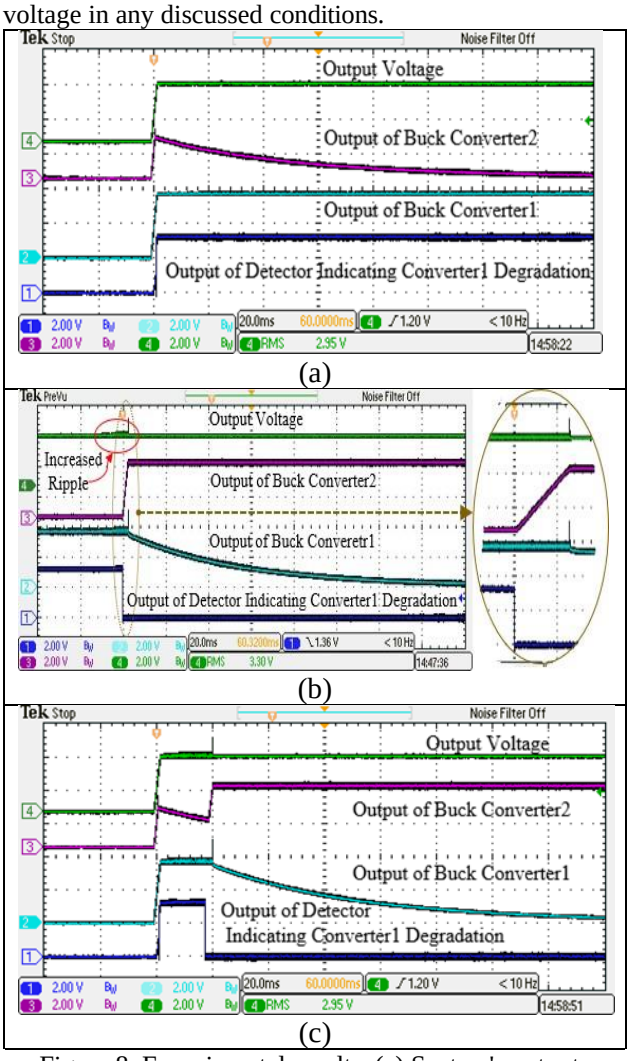


Figure 8. Experimental results. (a) System's outputs during turn-ON and upon healthy operation. (b) System's outputs upon fault occurrence during operation. (c) System's outputs during turn-ON while Buck Converter1 is degraded.

In this proposed solution care is taken to avoid false triggering by introducing additional delay unlike in available fault-tolerant techniques using signal processing-based fault detection. Table 3 lists a comparative analysis of the proposed system with available literature (Table 3 is provided in page 8 of the manuscript). From Table 3, we can observe that most available systems have either a redundant system always active or there is interruption time while switching from primary to a redundant system. The proposed system overcomes both of these issues. The proposed solution also has low design complexity with minimal additional components.

To summarize, the proposed solution provides a fault-tolerant buck power converter with zero interruption time. The proposed solution of fault-tolerance is conveniently expandable to MOSFET or diode degradation-induced failures. It is also applicable to other voltage converter topologies like boost, and buck-boost converters.

5. CONCLUSION

In this paper, a novel fault-tolerant buck converter system for critical power supplies is discussed. The increase in the ripple at the constant output of AEC is considered as primary health indicator. By online monitoring of the capacitor ripple and comparing it with the predefined threshold for AEC degradation a reconfiguration technique is proposed. The proposed system gives constant uninterrupted DC power by prognostically identifying primary buck converter failure and thereby activating secondary buck converter using signal processing technique. Here, false alarms are avoided by careful design. Also, a redundant secondary system is activated only after identifying primary converter failure. This reduces power wastage in the system and enhances the overall lifetime of the system. The system is simple in design, cost-effective, uses less number additional components, and is highly efficient. These qualities make the system suitable for numerous critical applications.

The proposed system is tested with simulations and experimentally. The results demonstrate the proclaimed properties of the system. The proposed system of fault detection and tolerance implementation is tested on a buck converter. However, this is scalable to other topologies of power converters like boost, and buck-boost efficiently. The fault detection and fault-tolerance implementation method introduced could be explored and adapted for the failure of buck converters due to MOSFET or diode degradation.

Reference	Converter Topology Considered	Faults Detected	Diagnostic Variable	Reconfiguration Strategy	Is redundant system/ element always active?	Complexity/ Cost	Is output uninterrupted?	Interruption Time
Kumar & Rajpurohit, 2020	Boost	OC/SC	output voltage	Bypass the faulty switch and Phase shift adjustment	Yes	Low	No	15ms
Jagtap & More, 2020	Buck, Boost, Buck-Boost	OC	Inductor Current	Inclusion of redundant component	No	Low	Yes, for Buck & No, for Boost &Buck - Boost	3us
Jagtap & More, 2020	Boost	OC	Inductor Current	Inclusion of redundant component	No	Low	No	93us for D=0.2, 4us for D=0.8
Xu & Chen, 2021	Boost, Buck - Boost	OC	Inductor Current	Bypass the faulty switch and Phase shift adjustment	Yes	Medium	No	Fast
Rahimi, et al., 2021	Boost	OC/SC	Inductor current	Inclusion of additional discrete components	Yes	Low	No	<<1Tsw
Soon, Lu, Peng, & Xiao, 2020	Buck	SC	Voltage across switch Vds	Inclusion of additional discrete components	No	Medium	No	10ms
Costa, Buticchi, & Liserre, 2017; 2018	Series Resonant DC-DC Converter	OC/SC	Inductor Current/Capacitor Voltage	Inclusion of additional discrete components	Yes	Medium	No	45ms
Li, Pan, Su, & Zhao, 2019	Buck	OC/Gain variation and Excess Noise	Inductor Current/ Capacitor Voltage	Inclusion of additional discrete components	Yes	High	No	10ms
Dhananjaya, M, Padmanaban, Almakhles, & Potnuru, 2021	Buck, Boost, Buck-Boost	OC/SC (partial)	Inductor Current/Input Voltage	Inclusion of Redundant Legs	Yes	Low	No	NA
Proposed System	**Buck**	**OC/S C**	**Ripple in the capacitor voltage**	**Inclusion of redundant leg**	**No**	**Low**	**Yes**	**Uninterrupted**

OC-Open Circuit, SC-Short Circuit, Tsw-1/Switching frequency, NA-Not available

Table 3. Comparative analysis of proposed system with existing systems

DECLARATIONS

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